DELHI TECHNOLOGICAL UNIVERSITY

MINUTES

of

35th Meeting

ACADEMIC COUNCIL

Date : 15.05.2023

Time : 11:30 A.M.

Venue : Vigyan Hall, 2nd Floor, Admin. Block, DTU

Shahbad Daulatpur, Bawana Road, Delhi-110042

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	vii. Minor Change in Criteria for Part Time Ph.D. Admissions for the Academic Year 2023-24. viii. Minor Change in Criteria for Full Time Sponsored M. Tech. Admissions for Academic Year 2023-24. ix. Minor Changes in Criteria for Industry/ Working Professionals in Ph.D. Programme for the Academic Year 2023-24. x. Ratification towards proposal of registration in 3rd Semester in M.Tech Program in r/o Mr. Shashank Khare (2K18/ENE/09).	
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DELHI TECHNOLOGICAL UNIVERSITY

Established under Govt. of Delhi Act 6 of 2009
(Formerly Delhi College of Engineering)
BAWANA ROAD, SHAHBAD DAULATPUR, DELHI-110042

No. F.DTU/Council/AC/Meeting/51/2022/744 Date : 12/6/023

Minutes of the 35th meeting of the Academic Council held on 15.05.2023 at 11:30 A.M. in Vigyan Hall, 2nd Floor, Admin Block, DTU, Delhi.

The following members were present:

1. Prof. J.P. Saini, Vice Chancellor, Delhi Technological University and Chairperson, Academic Council.
2. Prof. D.P. Goyal, Director, Indian Institute of Management, Shillong, Meghalaya (online)
3. Prof. Neharika Vohra, IIM Ahmedabad & Former Vice Chancellor, Delhi Skill & Entrepreneurship University, Dwarka, Delhi (online)
4. Prof. Bhim Singh, Electrical Engineering Department, Indian Institute of Technology, Delhi (online)
5. Prof. B.R. Chahar, Professor, Civil Engineering, Indian Institute of Technology, Delhi (online)
6. Sh. Rajesh Mathur, Advisor, Environmental Systems Research Institute (FICCI nominee).
7. Prof. Pragati Kumar, Dean, Industrial Research & Development & Head (EE)
8. Prof. Rinku Sharma, Dean Academic (PG)
9. Prof. Nirendra Dev, Dean, Planning & Consultancy
10. Prof. Rajeshwari Pandey, Dean Academic (UG)
11. Prof. Pravir Kumar, Dean, International Affairs & Head, Biotech.
12. Prof. S. Indu, Dean, Student Welfare
13. Prof. A.K. Srivastava, Dean, Outreach & Extension Activities
14. Prof. Rajesh Rohilla, Dean, Alumni Affairs & Head (T&P)
15. Prof. V.K. Minocha, Head, Civil Engineering Department
16. Prof. S. K. Garg, Head, Mechanical Engineering Department
17. Prof. Ruchika Malhotra, Head, Software Engineering Department
18. Prof. Dinesh Vishwakarma, Head, Deptt. of Information Technology
19. Prof. Vinod Kumar, Head, Computer Science & Engineering Deptt.
20. Prof. O.P. Verma, Head, Electronics & Communication Department
21. Prof. Ranganath M. S., Head, Department of Design
22. Prof. Vinod Singh, Officiating Head, Applied Physics Department
23. Prof. Anil Kumar, Head, Applied Chemistry Department
24. Prof. Nand Kumar, Head, Department of Humanities
25. Dr. Archana Singh, Head, Delhi School of Management
26. Prof. Amit Mookerjee, Head, University School of Management and Entrepreneurship (USME)
27. Ms. Divya Narayan, Head, Computer Centre

28. Sh. Kamal Pathak, Controller of Examinations
29. Prof. Reeta Wattal, Professor, Mechanical Engineering Department
30. Dr. M. Jayasimhadri, Assistant Professor, Applied Physics
31. Prof. Madhusudan Singh, Registrar and Member Secretary, Academic Council, DTU.

Following faculty also joined the meeting:

1. Prof. Raju Sarkar, Associate Dean (Academic- PG)
2. Prof. Priya Mahajan, Associate Dean (Academic- UG)
3. Prof. Girish Kumar, CEO, DTU-IIF
4. Prof. Rishu Chaujar, Applied Physics Deptt.
5. Prof. K.C. Tiwari

Agenda 35.1 : Opening Remarks by the Chairperson.

The Chairperson welcomed all the members to the 35th meeting of the Academic Council of Delhi Technological University. He stated that the University has started the implementation of various provisions of National Education Policy (NEP) 2020. Establishment of a separate Research and Development (R&D) Cell, International Student Office, Alumni Office, IPR Cell have already been established under NEP 2020.

Chairperson/ Vice Chancellor informed that in the academic year 2022-23 (till 17th April 2023) a total of 300 companies have made 1974 job offers to students from various streams of UG & PG programs in diverse fields of engineering and technology.

- Highest Package at Rs. 82.05 LPA (Atlassian).
- Average Package is Rs. 15.29 LPA.

The top recruiters include Google, Microsoft, Apple, Intel, Samsung, Qualcomm, Texas Instruments, Maruti, Tata Motors, GAIL, EIL, Goldman Sachs, Morgan Stanley, BAIN, Mckinsey, KPMG, PwC and many more similar organizations. Also 107 companies have offered internship to more than 350 students with average stipend of Rs. 76000/-. Highest stipend of Rs. 2 Lacs per month offered by Sprinklr.

Currently 56 start-ups are incubated/ pre-incubated in DTU-IIF. A total of 35 start-ups have been incorporated in form of companies by the efforts of IIF centre.

Agenda 35.2 : Confirmation of the minutes of the 34th meeting of Academic Council held on 14.12.2022.

The minutes of the 34th meeting of Academic Council held on 14.12.2022 were circulated among all the members vide no. F.DTU/ Council/ AC/ Meeting/ 41/ 2022/ 404 dated 23.12.2022. A copy of the minutes of 34th meeting was placed in agenda annexure.

No comments were received from any of the members.

Decision : The Academic Council confirmed the minutes of 34th meeting of the Academic Council.

Agenda 35.3 : Action taken report on the decisions taken in the 34th meeting of the Academic Council.

Action Taken Report on the decisions taken in the 34th meeting of the Academic Council held on 14.12.2022 is as below:

S. No.	Agenda Item	Decision	Action Taken by Council Branch	Compliance Report
34.1	Opening Remarks by the Chairperson.	Points mentioned are taken on record.	Noted.	Matter of record.
34.2	Confirmation of the minutes of the 33rd meeting of Academic Council held on 16.08.2022.	The Academic Council confirmed the minutes of 33rd meeting of the Academic Council.	Noted.	Matter of record.
34.3	Action taken report on the decisions taken in the 33rd meeting of the Academic Council.	The Academic Council took the Action Taken Report on 33rd AC meeting on record.	Noted.	Matter of record.
34.4	Adoption of (i) UGC Guidelines for allowing students to pursue two academic programs simultaneously and (ii) UGC Regulations for Academic Collaboration between Indian and Foreign Higher Educational Institutions to offer Twinning, Joint Degree and Dual Degree Programmes, Regulations, 2022.	The Academic Council deliberated and approved the proposal in principle. The Academic Council also constituted a committee of the following to review the guidelines including financial part of the proposal and suggest procedure for admission, fee structure, exit option and training & placement scope etc. – 1. Dean, International Affairs – Chairperson 2. Dean Academic (UG) 3. Dean Academic (PG) 4. Dean, IRD 5. Dean, Student Welfare 6. Head of the Department of Design 7. Head, USME 8. Controller of Examinations The committee may opt or take help of Prof. Bhim Singh of IIT Delhi as in IIT Delhi such provisions are already there. The recommendations of the committee may be placed in the next meeting of Academic Council.	Decision conveyed to Dean Academic (UG) vide letter no. 3513 dated 05.01.2023.	A meeting was held on 20.01.2023 with all committee members in the Dean (IA) office. Committee members have unanimously suggested and agreed on a broad frame-Work to implement UGC suggested dual, double and twinning programmes.

34.5	Approval for inclusion of a clause of linking a fraction of Class Work Sessional (CWS) marks with attendance in Regulation R.1(B). 22.	The Academic Council considered and approved for awarding 5 marks towards attendance of the student in each course as per given table and inclusion of the same as a clause in Regulation R.1(B).22 in Class Work Sessional (CWS) applicable to both UG and PG students. The Council also advised to have effective and operational ERP for attendance of the students.	Decision conveyed to Dean Academic (UG) vide letter no. 3512 dated 05.01.2023.	Notified vide letter no. F.105(971)DTU/ Acad-UG/ 2022-23/12046-52 dated 05.01.2023.
34.6	Approval for Academic Calendar for AY 2022-23 Even Semester for students of UG and PG programmes (except for B.Tech/BA/BBA/MA (Eco) 1st year students).	The Academic Council considered and suggested to review the Academic Calendar for AY 2022-23 (Even Semester) for students of UG and PG programmes. The Council advised to place the revised Academic Calendar before the Vice Chancellor for approval.	Decision conveyed to Dean Academic (UG) vide letter no. 3511 dated 05.01.2023.	Notified vide letter no. F.105(641)DTU/ Acad-UG/ 2018-19/11964-72 dated 28.12.2022.
34.7	Provision of earning at least 4 credits from NPTEL/ SWAYAM platforms if a student is opting for 8 credits through MOOCs platforms.	The Academic Council considered and appointed a committee consisting of Dean Academic (UG) as Chairperson with Dean Academic (PG), Prof. Neeta Pandey, Coordinator, MOOC and HOD (Training & Placement) as members to suggest guidelines for allowing to pursue more credits through equivalent MOOC/SWAYAM courses against FEC/GEC courses. The committee will submit its recommendations to the Vice Chancellor for approval.	Decision conveyed to Dean Academic (UG) vide letter no. 3510 dated 05.01.2023.	A committee has been constituted vide letter no. F.105(937)DTU/ Acad-UG/ 2021-22/12410-46 dated 09.01.2023.
34.8	Syllabus Revision for EC457 Natural Language Processing.	The Academic Council considered and approved the revised syllabus for EC457 Natural Language Processing and also advised that list of books attached should be revised and updated.	Decision conveyed to Dean Academic (UG) vide letter no. 3509 dated 05.01.2023.	Notified vide letter no. F.105(621)DTU/ Acad-UG/ 2018.-19/ 12240-44 dated 13.01.2023.

34.9	Approval for starting a certificate program on "Basic Python Programming" for underprivileged students.	The Academic Council considered and approved for starting a certificate program on "Basic Python Programming" for underprivileged students in principle with the condition that no additional manpower will be provided for this purpose and this course should be conducted on lab on wheels. The Academic Council also advised that the course will be coordinated by the Dean, Outreach & Extension Activities.	Decision conveyed to Dean (O&EA) vide letter no. 3498 dated 05.01.2023.	Certificate program on "Basic Python Programming" for underprivileged students has been started.
34.10	Approval for change in course codes of Discipline Specific Electives of the BBA Program, USME.	The Academic Council considered and approved for changes in course codes of Discipline Specific Electives of the BBA Program, USME.	Decision conveyed to Head, USME vide letter no. 3497 dated 05.01.2023.	The change in course code has been Implemented.
34.11	Approval for Guidelines for Engaging Professor of Practice in Delhi Technological University.	The Academic Council considered and approved the Guidelines for Engaging Professor of Practice in Delhi Technological University.	Decision conveyed to all Deans vide letter no. 3494 dated 05.01.2023.	Implemented.
34.12	Approval for minor modifications in the contents of the course Electromechanical Energy Conversion and Transformers (EE-205) & Asynchronous and Synchronous Machines (EE-208).	The Academic Council considered and approved minor modifications in the contents of the course Electromechanical Energy Conversion and Transformers (EE-205) & Asynchronous and Synchronous Machines (EE-208) with the advice that list of books should be reviewed and updated.	Decision conveyed to Head, Deptt. of Electrical Engg. vide letter no. 3502 dated 05.01.2023..	Implemented.
34.13	Approval for minor modifications in the contents of the course Digital Circuits and Systems (EE-204).	The Academic Council considered and approved the minor modifications in the contents of the course Digital Circuits and Systems (EE-204) with the advice that list of books should be reviewed and updated.	Decision conveyed to Head, Deptt. of Electrical Engg. vide letter no. 3503 dated 05.01.2023..	Implemented.
34.14	Approval for minor modifications in the contents of the course Power System Analysis (EE 304) & Power Transmission and Distribution (EE 303).	The Academic Council considered and approved minor modifications in the contents of the course Power System Analysis (EE 304) & Power Transmission and Distribution (EE 303) with the	Decision conveyed to Head, Deptt. of Electrical Engg. vide letter no. 3504 dated 05.01.2023..	Implemented.

		advice that list of books should be reviewed and updated.		
34.15	Proposal for addition of new course Probability and Random Process (EE 334) in VI Semester.	The Academic Council considered and deferred this proposal. The Council advised that an Interdisciplinary Committee under Dean (IRD) of the University should examine this issue in detail to ensure that new courses to be introduced in any department are not being taught in other department with similar title and contents. This will ensure the optimal utilization of University resources in terms of manpower as well as infrastructure.	Decision conveyed to Head, Deptt. of Electrical Engg. vide letter no. 3505 dated 05.01.2023..	No action required.
34.16	Proposal for addition of new elective course Fundamentals of Machine Learning (EE 336) in VI Semester.	The Academic Council considered and deferred this proposal. The Council advised that an Interdisciplinary Committee under Dean (IRD) of the University should examine this issue in detail to ensure that new courses to be introduced in any department are not being taught in other department with similar title and contents. This will ensure the optimal utilization of University resources in terms of manpower as well as infrastructure.	Decision conveyed to Head, Deptt. of Electrical Engg. vide letter no. 3506 dated 05.01.2023..	No action required.
34.17	Proposal for Mandatory Publication Requirement for Award of Ph.D. Degree – Discipline of Design.	The Academic Council considered and deferred this matter. The Council advised that such matters should be first examined by Dean Academic (PG) and after taking approval of competent authority, matter should be placed before Academic Council.	Decision conveyed to Head, Deptt. of Design vide letter no. 3499 dated 05.01.2023.	To be re-submitted for consideration and approval of Academic Council.
34.18	Proposal for adding specialization in Master of Design (M.Des.) programme in Department of Design from 2023-24 onwards.	The Academic Council considered and deferred this matter. The Council advised that such matters should be first examined by Dean Academic (PG) and after taking approval of competent	Decision conveyed to Head, Deptt. of Design vide letter no. 3500 dated 05.01.2023.	To be re-submitted for consideration and approval of Academic Council.

		authority, matter should be placed before Academic Council.		
34.19	Proposal for adding specialization in Bachelor of Design (B. Des.) program in Department of Design from 2023-24 onwards.	The Academic Council considered and deferred this matter. The Council advised that such matters should be first examined by Dean Academic (UG) and after taking approval of competent authority, matter should be placed before Academic Council.	Decision conveyed to Head, Deptt. of Design vide letter no. 3501 dated 05.01.2023.	To be re-submitted for consideration and approval of Academic Council.
34.20	Approval for change of courses offered by DSM in minor basket for B. Tech students.	The Academic Council considered and approved for change of courses offered by Delhi School of Management in minor basket for B. Tech students.	Decision conveyed to HOD, DSM vide letter no. 3491 dated 05.01.2023.	Implemented.
34.21	Approval for provision of allowing additional credits over prescribed credits of B. Tech Degree to complete Minor in a specific discipline.	The Academic Council considered and approved in principle the provision of allowing additional credits over prescribed credits of B. Tech Degree to complete minor in a specific discipline. The Council advised that this matter should also be examined by a committee of the following: 1. Dean (IRD), Chairperson 2. Dean Academic (UG) 3. Dean Academic (PG) 4. Dean, Student Welfare The final recommendations of the committee shall be placed before the Vice Chancellor for approval.	Decision conveyed to Dean Academic (UG) vide letter no. 3508 dated 05.01.2023.	Committee to review the matter is notified vide letter no. F.105(823)DTU/ Acad-UG/ 2021-22/ 12111-12 dated 06.01.2023.
34.22	Matter for ratification. i. Admissions in Ph.D. Program for Industry/Working Professionals. ii. Promulgation of DTU Innovation and Startup Policy. iii. Admission Brochure for Ph.D. program for the Academic session: January 2023. iv. 1st year B. Tech. Academic calendar 2022-23.	The Academic Council ratified the 4 actions taken by the University.	Noted	Matter of record.

34.23	Matter for information. i. Admissions made in Ph.D. program for the summer session August 2022 (International, QIP and ADF). ii. Formal registration to Ph.D. students upon successful completion of course work and comprehensive examinations and approval of research Plan by respective DRCs. iii. Cancellation/Withdrawal of admission during August 2022 to November 2022 from Ph.D. program. iv. Admissions made in Master of Technology (M. Tech.), Master of Design (M. Des.), Master of Science (M. Sc.), Master of Business Administration (MBA) and Master of Economics (MAE) programs for the session 2022-23. v. Admissions under various UG programs in AY 2022-23. vi. Admissions in B.Tech program in AY 2021-22	Academic Council noted the information.	Noted	Matter of record.
34.24	Any other item with the permission of the Chair.	No other item.	Noted.	Matter of record.
S.A. 34.25	Approval for revision of Guidelines for Industrial Visits	The Academic Council advised Dean, Student Welfare to place the matter in the Finance Committee by sending a proposal on the subject to Controller of Finance. Academic Council advised that point 5 of the guidelines in the above Agenda making industrial visit mandatory shall not be included.	Decision conveyed to Dean Academic (SW) vide letter no. 3507 dated 05.01.2023.	Implemented.
S.A. 34.26	Matter of ratification-Mandatory publication requirement for award of Ph.D degree.	Academic Council ratified the action taken by the University.	Decision conveyed to Dean Academic (SW) vide letter no. 3495 dated 05.01.2023.	Matter of record.

S.A. 34.27	Adoption of National Educational Policy (NEP) 2020 notified by the Ministry of Education, Govt. of India by Delhi Technological University.	The Academic Council approved for Adoption of National Educational Policy (NEP) 2020 notified by the Ministry of Education, Govt. of India by Delhi Technological University. (Copy of NEP 2020 is placed at Annexure pages 78 to 143).	Decision conveyed to Prof. K.C. Tiwari, Deptt. of Civil Engg. vide letter no. 3496 dated 05.01.2023.	Dean(IRD) is appointed as nodal officer for implementation of different provisions of NEP 2020. Provisions of NEP 2020 have been started for implementation.

Decision : The Academic Council took the Action Taken Report on its 34th meeting on record.

Agenda 35.4 : To review the fee structure and changes in eligibility criteria for Post Graduate (M.Tech) admissions for the academic year 2023-24.

It was submitted that as per 33rd Academic Council decision vide Agenda number 33.5, the council constituted the following committee to review the fee structure and other modalities of Post Graduate (M.Tech.) Admissions.

Committee members are as under:

1.	Prof. S.K. Garg	Chairperson
2.	Prof. Nirendra Dev	Member
3.	Prof. K.C Tiwari	Member
4.	Dean (PG)	Member-Secretary

The recommendations of the committee were as under:

1. Any unfilled GATE scholarship seat will be offered to the candidates without GATE score and without any AICTE or DTU scholarship on the basis of Admission test.

2. In view of the National Education Policy, 2020 (NEP,2020) lays emphasis on interdisciplinary nature of the courses & programme(s), the additional branches may be added to qualifying degree and Gate Subjects in the departments which are interdisciplinary in nature so as to create an interdisciplinary culture in M.Tech. programmes.

   Action Taken: *In this regard, the information has been sent to the Departments vide Circular No. 104-45/Acad-PG/M. Tech. Circular/2021/159-166 (Copy attached) and also incorporated in the upcoming Admissions and also mentioned in the Admission Brochure 2023-24.*

3. The **Non-GATE** candidate(s) are not eligible to receive any AICTE scholarship/ fellowship in any of the M.Tech. programme(s). Therefore, it is proposed that the University may consider to provide financial assistance of Rs. 7500/- per month based on the recommendations of a committee constituted by the Competent Authority. The Committee constituted by the University shall examine cases for awarding Scholarship to Non-Gate students based on performance & requirements in the respective departments. The proposed terms & conditions for providing financial assistance to Non-GATE candidate(s) admitted in M.Tech. programme(s) are as under:
   a. Candidates getting financial support under DTU-TA must not be getting/claiming any financial support/stipend in any form from any sponsoring agencies. If the candidate does any paid internship, then this financial support under DTU-TA will terminate.

b. Financial assistance in the form of teaching assistantships (referred to as DTU Teaching Assistantship (DTU-TA) is offered to the M. Tech. students and will be awarded semester-to-semester basis for a maximum of four semesters or till the final submission of M Tech Dissertation. These candidates will be required to take academic work load of 6-8hours as assigned by the department such as laboratory classes, tutorials, seminars, research projects or any other work etc. along with their regular academic work related to their own degree programme.
c. The stipend for the assistantship shall be paid at the approved rates as notified by the University from time to time.
d. In case of unsatisfactory performance of the candidate in discharging the academic duties assigned by the department or poor academic performance, the University may discontinue the financial assistance on the recommendation of concerned Head of the department.
e. The University reserves the right to terminate the DTU-Teaching Assistant(TA) anytime without any notice on unsatisfactory report of the assigned work / teaching duties carried out by the candidate.

It was also submitted for information that the recommendations of the duly constituted committee were placed before the Finance Committee in its 29th meeting held on 07.02.2023. The Finance Committee considered and recommended that- *"No change in current fee structure of M.Tech. program should be made and other modalities as placed be incorporated and further recommends the agenda to the Board of Management for its approval"*.

Further, the committee also recommended that the timeline of the admission will be shorten and admission process shall be done in a time bound manner; the gap between two consecutive rounds should be minimum; the counselling should be done a department level in the physical mode where the number of applications are less than five time the number of seats. All the applicants may be called in the first round itself. Even where the application are more than five times, the gap between two consecutive rounds should not be more than three days. This will be ensuring that the number of withdrawals are minimum and the university will be in a position to retain the right candidates.

Decision : **The Academic Council considered and approved the provisions for admissions of Non-Gate score candidates against vacant seats through written test at University level and also providing stipend/financial assistance of Rs. 7500/- to the candidates who are admitted without GATE score on the basis of recommendation of committee constituted by the University. The committee shall examine the performance of student seeking the financial assistance and also requirement of teaching assistance in the department. The Council also approved the changes in eligibility criteria for admissions in Postgraduate (M.Tech) programs for the academic year 2023-24.**

Agenda 35.5 : Approval for course work credit transfer in Ph.D program at DTU.

It was submitted to the Academic Council that as per the approval of the Hon'ble VC, a committee comprising following members has been constituted to frame the policy/guidelines for course work credit transfer in r/o Ph.D. programme(s).

1.	Prof. Pragati Kumar, Dean (IRD)	Chairperson
2.	Prof. S. Indu, Dean (DSW)	Member
3.	Prof. Dinesh Kr. Vishwakarma, Chief Warder	Member
4.	Prof. Ram Singh, Deptt. of Applied Chemistry	Member
5.	Dr. Sonal Thakral, Asstt. Professor	Member Secretary

The recommendations of the Committee have already been approved by the Competent Authority which are as under:

1. The University shall have a policy of accepting transfer of credit earned by a student from Indian or Foreign Universities/Educational Institutions/Research Institutions with which the University has signed an MOU for students and faculty exchange, and any such institution approved by the Competent Authority for the purpose of credit transfer, on the recommendation of the DRC of the concerned department.

2. Request for acceptance of transfer of credits to DTU shall be:
   a. entertained only if received from such candidates who have been duly selected for admission in Ph.D Programme, as per the rules and regulations governing admission in the University.
   b. made by the student concerned within 10 days from the date of his/her course registration in the appropriate semester before the DRC of the respective department duly forwarded by the concerned supervisor. The DRC will submit the application with recommendations to the Competent Authority for approval.

3. The Dean PG shall be the coordinating officer for receiving and processing the request for accepting the transfer of credits. To facilitate and expedite the process, the Dean may constitute a Committee comprising of a senior faculty as Chairman, two faculty members and finalise the request for acceptance of credit.

4. The maximum credits that can be accepted for transfer shall not exceed 25% of the total credits of the mandatory credits required for completing the Ph.D degree.

5. In specific cases credits exceeding 25%, may be permitted by special approval of the Competent Authority.

6. The credit transfer shall not be allowed for more than **50%** of mandatory requirement of credits for Course work.

7. Only such courses may be considered for acceptance of credit transfer, in which the students have secured at least B grade/equivalent GPA/a minimum of 50% marks, as the case may be.

8. The credit equivalence for accepting credit transfer shall be determined as under:
   a. for credit(s) earned by students from Universities that have the credit system in place, a Course work requiring 15 contact hours shall be considered as equivalent to 1 credit of the University; and
   b. for Courses completed from Universities/ Educational Institutions/ Research Institutions that do not follow credit system but have semester system in place, a Course work requiring a minimum 30 lecture hours per semester shall be considered as equivalent to 2 credits of the University; and
   c. for Courses completed from Universities/ Educational Institutions/ Research Institutions that neither follow the credit system nor have the semester system, a Course requiring formal classroom instruction and/or lab work of at least 2 hours per week shall be considered as equivalent to 2 credits of the University.

9. The above policy of credit transfer will be impugned with Policy of credit transfer of B.Tech. /M.Tech. programme in terms of kind of institutes.

Decision : The Academic Council considered the agenda but deferred for further deliberations on transfer of credit of course work completed by the Ph.D. students in other University/ Institution.

Agenda 35.6 : Approval for Approval for introducing MOOC courses in Ph.D program course work.

It was submitted to the Academic Council that as per DTU Ph.D. Ordinance R. 6.2: "The credit assigned to Ph.D. course work shall be a minimum of 08 credits and a maximum of 16 credits". Requirement of credits based on Educational Qualification for completion of course work is as under:

Degree	Minimum Credits required	Distribution of credits
M.Tech./MBA or M.Sc./MA with M.Phil	8	4 credit = Research Methodology (Mandatory) Non Credit = Research and Publication Ethics (Mandatory and Qualifying Course) 4/8/12 credit = earned by opting subject specific course
M.A./M.Sc.	12	
B. Tech	16	

As per UGC regulation for PhD 2022 R. 9.1 "The Credit requirement for the Ph.D. coursework is a minimum of 12 credits, including a "Research and Publication Ethics" course as notified by UGC vide D.O. No. F.1-1/ 2018(Journal/ CARE) in 2019 and a research methodology course. The Research Advisory Committee can also recommend UGC recognized online courses as part of the credit requirements for the Ph.D. programme".

To provide learning support to students, it is proposed that the MOOC courses inline of UG and PG programme should be implement in Ph.D. programme also for completion of course work credits through online learning platforms.

In view of above, the proposal is as under:

Credit	Course	Proposed Mode	Remarks
4	Research Methodology	**Physical /Online**	Proposed to complete credits online MOOC courses through SWAYAM/ NPTEL and for subject specific course, department must ascertain the relevance of subject duly approved by the BOS/DRC of the concerned Department.
0	Research and Publication Ethics	**Physical /Online**	
4/8/12	Subject Specific Course	**Physical/Online**	

Decision : The Academic Council considered and approved for allowing MOOC courses in Ph.D program against course work.

Agenda 35.7 : To consider the recommendation of committee on the Revision of B. Tech Curriculum to align its credit framework with NHEQF and introduce the provision of multiple-entry and multiple-exit in accordance with NEP 2020.

It was submitted to the Academic Council that the Delhi Technological University offers B. Tech programme in 14 disciplines with most modern curricula, based on the Choice Based Credit System (CBCS), having rich mix of courses from science, engineering, management, social sciences, humanities, fine arts, liberal arts, classical music, sports, etc. The course curricula have been developed with a view to integrate advancements in science and engineering, while also incorporating industry relevant technologies.

The University has started the implementation of various provisions of the NEP 2020. The provision of multi- disciplinarily has been implemented in the University where in, a student can get a Minor degree in any other discipline along with his Major specialization. The first batch of students under this provision shall be passing out in year 2023. Other innovative features like credit transfers, earning of credits through MOOCs, Internship in industry, value added courses/ ability enhancement courses are already implemented. The details of major curriculum revision for B. Tech. programmes since 2015 are presented below:

Year of Revision	Revision Details
2015	Major changes in Scheme of Examination including continues assessment and introduction of grading pattern. Reference: 11th AC meeting held on 24.06.2015 agenda items 11.10 & 11.16
2018	Introduction of choice based credit system and Foundation Elective Courses in the curriculum. Reference: 18th meeting held 20.04.2018, agenda item 18.7
2020	Provision of MINOR was introduced as a part of multidiscipline learning and learning beyond the curriculum of the program to which the student is admitted. Reference: 25th meeting held on 04.11.2020, agenda items 25.12, 25.13, 25.14, 25.15

A committee was constituted by the Vice Chancellor under the chairmanship of Dean (Academics-UG) vide office order no. 105(922)/ DTU/ Acad-UG/ ACA/ 2021-22/ 14145-52 dated 28.05.2022, to review the existing curriculum to align its credit framework with NHEQF and introduce the provision of multiple-entry and multiple-exit in all its programmes. Various meetings of the committee were convened to deliberate on these aspects of NEP 2020. After due deliberations, the committee unanimously recommended the New Scheme to be applicable for B.Tech students admitted from AY 2023-24 onwards as placed at ***Annexure pages ... to ....***

Decision : The Academic Council considered and suggested changes in the 1st year scheme and authorized the Vice Chancellor to consider the revised scheme along with re-look on the requirement of credits for award of minor area of study. The revised B.Tech curriculum in line with the NEP 2020 and NHEQF shall be applicable w.e.f. academic year 2023-24.

The Council also suggested that academic departments shall prepare syllabi as per revised schemes through organizing BoS meetings and course curriculum development workshop with external members.

Agenda 35.8 : Provision of earning maximum of 16 credits through MOOC platforms.

It was submitted to the Academic Council that the scheme of B.Tech program offers flexibility of pursuing 8 credits courses through MOOCs from online platforms SWAYAM, NPTEL, Coursera, Edx or from other higher education institutions such as IITs etc. The provision of earning credits through MOOCs was introduced in AY 2018-19. As per existing guidelines a student is allowed to earn 8 credits (2 elective courses of 4 credits each) from MOOCs and for each 4 credits, student has to opt for 2 MOOCs. No formal examination is conducted for MOOC based courses for the students and the grades as awarded by the MOOC platform are transferred in the transcript.

As per NEP 2020, upto 40% of the courses may be offered in online learning mode. In view of the above and citing the fact that many students are not able to complete their Minor in a specific domain due to registration limitations in various courses required for completing the Minor degree, it is proposed that students admitted in AY 2021-22 onwards may be allowed to earn maximum of 16 credits through MOOC platform as per following details:

1. Students may be allowed to take maximum of 12 credits through MOOC for DEC/GEC.

2. Students may be allowed to take maximum of 4 credits through MOOC for FECs. FECs through MOOC may be allowed from 2nd semester onwards.

Out of the 16 credits, student is earning through MOOC for DEC/ GEC/ FEC, at least 08 credits must be earned through NPTEL/SWAYAM.

Decision : The Academic Council considered and approved the provision of earning maximum of 16 credits through MOOC platforms out of which 4 credits against FEC/SKC/AEC courses and remaining 12 credits for DCE/GEC courses.

Agenda 35.9 : Approval for Establishment of "Vinod Dham Centre of Excellence for Semiconductors and Microelectronics" in DTU.

It was submitted to the Academic Council that as the world continues to reel from a dearth of semiconductors, it has become extremely vital to secure supply chains from geopolitical risks and natural disasters. While the Covid-19 pandemic may have exacerbated the demand-supply imbalance in chips, the signs of an impending crisis had appeared long before the pandemic. Apart from negative variables like the U.S.-China trade war, the concentration of advanced manufacturing capabilities in the hands of a few players had significantly constricted the entire value chain. To build resilience in the future, it will be important to identify and mitigate potential disruptions to the semiconductor industry. More broadly, there is a pressing need to look beyond microchips and anticipate threat factors for the electronics industry and other allied sectors.

Hence, Delhi Technological University has established a Vinod Dham Centre of Excellence for Semiconductors and Microelectronics in order to support Government of India's vision to build a vibrant Semiconductor and Display Ecosystem enabling India's emergence as a global hub for electronics manufacturing and design. The Centre will help in developing a semiconductor and display eco-system for transformation from a wafer to chips to start-ups. State-of-the-art facility for training, fabrication & testing will be created to carry out interdisciplinary research in Semiconductor technologies, Microelectronics and associated areas. The Centre has been established to impart training & research in thrust area of Semiconductor Technology and IC Manufacturing; and also provide a platform to boost productivity, address emerging skill gaps and align training & research with industry needs. The main objectives of the Centre include:

Objectives:

1. To establish a centralized state of the art infrastructure facility for next generation device design/materials research/fabrication and sustain educational resources for cutting edge Research and Development in Semiconductor and Microelectronics.
2. Capacity building in terms of skilled manpower at different levels such as technicians, supervisors and engineers in the area of Semiconductor Technology, IC Manufacturing and Microelectronics.
3. Design the curriculum with desired skill sets in research, design, fabrication, equipment manufacturing, packaging, and other related fields for development of Indian semiconductor and display ecosystem.
4. To offer internship opportunities to the students of degree, diploma and certificate level institutions at state and national levels under Govt of NCT of Delhi.

5. Collaboration between Delhi Technological University and Semiconductors/Microelectronics Industry in order to align training & research as per industry needs.

Vinod Dham, a DCE alumnus and popularly known as the Father of Pentium Chip has committed to fund and support DTU with an amount of Rs. 1 Crore to establish this Centre of Excellence for Semiconductors and Microelectronics which is in line with the India Semiconductor Mission to deal with the global shortage of semiconductor chips. Out of this, an amount of 50,000 USD (In first phase) has already been received in the account of DTU for VDCoE4SM for starting the activities of the Centre,

It was noted, the Board of Management, DTU had approved the guidelines for the creation of Centre for excellence in DTU vide its resolution number 41.4 dated 01.03.2021 and the said proposal is in the line of DTU guidelines for creation of Centre of Excellence.

The detailed proposal for the Establishment of Vinod Dham Centre of Excellence for Semiconductors and Microelectronics (VDCoE4SM) at Delhi Technological University (DTU) is placed at ***Annexure pages ... to ....***

Decision : The Academic Council considered and approved for Establishment of "Vinod Dham Centre of Excellence for Semiconductors and Microelectronics" as an independent centre with all academic and administrative control. Vinod Dham Centre of Excellence will not be a part of any other department.

Agenda 35.10: Approval for introduction of a Minor in Semiconductors and Microelectronics for B.Tech students under the "Vinod Dham Centre of Excellence for Semiconductors and Microelectronics".

With reference to the Office Order No. Phy/DTU/Office Order/158/2023 dated January 18, 2023, a workshop of the following committee members was held on February 20, 2023 in Room No. 307, Admin Block-2nd Floor to review the PG/UG Level Advanced Semiconductors programme planned to be proposed under the Vinod Dham Centre of Excellence for Semiconductors and Microelectronics.

The following committee members and external experts attended the meeting:

1. Prof. Rishu Chaujar, Dept. of AP : Coordinator
2. Prof. Pragati Kumar, Dept. of EE : Member
3. Prof. A. Srinivas Rao, Dept. of AP : Member
4. Prof. Rajeshwari Pandey, Dept. of ECE : Member
5. Prof. Neeta Pandey, Dept. of ECE : Member
6. Prof. Dinesh Chutani, Dept. of ECE : Member
7. Prof. Suresh C. Sharma, Dept. of AP : Member
8. Prof. Mini Sreejeth, Dept. of EE : Member
9. Prof. R. P. Sharma, IITD : External Expert
10. Prof. R. S. Gupta, GGSIPU : External Expert
11. Prof. Mridula Gupta, DU : External Expert
12. Dr. Navneet Kaushik, ST Microelectronics : External Expert
13. Dr. Janesh Kaushik, SSPL, DRDO : External Expert
14. Suggestions and advice from Sh. Vinod Dham (Online Expert)

After detailed discussion, deliberation(s) and review of the UG/PG Level programme planned to be proposed under the Vinod Dham Centre of Excellence For Semiconductors and Microelectronics, the following recommendation has been proposed:

1. In order to enhance the semiconductor manufacturing skills and increase the spectrum of students pursuing course in Semiconductors so as to build a strong semiconductor and display ecosystem, the following is proposed from the upcoming academic session for the students of B.Tech programmes:

   A Minor in Semiconductors and Microelectronics for B.Tech students as per the scheme of minor in the University Curriculum where a student will opt for 6 courses of 4 credits each from a basket of courses for Semiconductors and Microelectronics as specified below:

Compulsory Courses (to attain a minor)		Elective Courses (any two)	
Course Code	Course Title	Course Code	Course Title
EPXXX	Advanced Semiconductor Device Physics	EC431	MEMs and Sensor Design
EPXXX	Compact Modeling and Process Simulation of Semiconductor Devices	EC415	System On Chip Design
EPXXX	Advanced Wafer Processing	EC408	Low Power VLSI Design
EPXXX	Advanced Chiplets Packaging and Reliability Engineering	EC419	Memory Design
		EPXXX	Semiconductor Optoelectronics
		EPXXX	Next Generation Semiconductor Materials

Note: The courses required to attain a minor are to be opted from the basket of elective courses as proposed in the curriculum by different departments.

The above Minor is proposed to come up under the Vinod Dham Centre of Excellence for Semiconductors and Microelectronics. The detailed syllabus of the said courses is placed at ***Annexure pages ... to ....***

Decision : The Academic Council considered and approved for introduction of a Minor in Semiconductors and Microelectronics for B.Tech students under the "Vinod Dham Centre of Excellence for Semiconductors and Microelectronics". The Council further advised that the proposal may be sent to different departments for their feedback on the courses offered and also segregate the mandatory courses and elective courses for the minor.

Agenda 35.11 : Approval for Four Year BBA Honours/BBA Honours with Research program.

It was submitted to the Academic Council that in the online meeting and subsequent discussion of the Board of Studies, USME, held on 7th May, 2023, the Four Year BBA Honours/BBA Honours with Research program was approved and recommended as Agenda item for the consideration of the Academic Council. Details are as under:-

Four Year BBA Honours/ BBA Honours with Research

The curriculum and structure for the Four Year BBA Honours/ BBA Honours with Research, as per the guidelines of the NEP and related UGC framework, is proposed for approval of the Academic Council. The Program includes core, minor, value added and skill enhancement courses, with internship and projects/dissertation, as per NEP guidelines, and also provides for multiple exit policy.

Finally, it will be offered only to newly admitted students, from the batch admitted in 2023-24, onwards.

It was noted that BBA Three Year program has been offered since 2017-18 academic session onwards.

Decision : The Academic Council considered and approved the Four Year BBA (Honours)/ BBA (Honours) with Research program with minor modifications in total credits requirement for award of BBA (Honours)/ BBA (Honours) with Research in line with NHEQF. The Council authorized the Vice Chancellor to approve the revised scheme suggested by the committee.

Agenda 35.12 : Approval for Four Year BA Honours/BBA Honours with Research in Economics program.

It was submitted to the Academic Council that in the online meeting and subsequent discussion of the Board of Studies, USME, held on 7th May, 2023, the Four Year BBA Honours/BBA Honours with Research in Economics program was approved and recommended as Agenda item for the consideration of the Academic Council. Details are as under:-

Four Year BA Honours/BBA Honours with Research in Economics

The curriculum and structure for the Four Year BA Honours/ BA Honours with Research, in Economics, as per the guidelines of the NEP and related UGC framework, is proposed for approval of the Academic Council. The Program includes core, minor, value added and skill enhancement courses, with internship and projects/dissertation, as per NEP guidelines, and also provides for multiple exit policy.

Finally, it will be offered only to newly admitted students, from the batch admitted in 2023-24, onwards.

It was noted that BA (Honours) Economics Three Year program has been offered since 2017-18 academic session onwards.

Decision : The Academic Council considered and approved the Four Year BA Honours in Economics program with minor modifications in total credits requirement for award of BA Honours/ BBA Honours with Research in Economics in line with NHEQF. The Council authorized the Vice Chancellor to approve the revised scheme suggested by the committee.

Agenda 35.13 : Approval for Four Year ITEP – Integrated Program in Teacher Education in the B.Com./B.Ed stream for the Secondary Education level program.

It was submitted to the Academic Council that in the online meeting and subsequent discussion of the Board of Studies, USME, held on 7th May, 2023, the Four Year ITEP – Intergrated Program in Teacher Education in the B.Com./B.Ed stream for the Secondary Education level program was approved and recommended as Agenda item for the consideration of the Academic Council. Details are as under:-

Four Year ITEP – Intergrated Program in Teacher Education in the B.Com./B.Ed stream for the Secondary Education level program

In principle approval is sought from the esteemed AC, for the initiation of the Four Year ITEP – Intergrated Program in Teacher Education in the B.Com., B.Ed stream for the Secondary Education level, under NCTE registration. Also approval is sought to explore the setting up of the School of Learning in future as per the requirement of NCTE in the matter, and as per the Norms and Standards notified in the relevant gazette notification and consistent with DTU norms, and as required by NCTE for launch of this program.

Decision : The Academic Council considered and deferred the proposal to introduce Four Year B.Com/ B.Ed program. The Council constituted a committee of following to review the proposal and re-submit to the Academic Council:

1. **Prof. Amit Mookerjee**
2. **Prof. Rajeshwari Pandey**
3. **Prof. Pragati Kumar**
4. **Prof. Rajan Yadav**

Agenda 35.14 : Approval of Syllabi for courses offered in the III and IV Semester, M.A. Economics.

It was submitted to the Academic Council that approval is also sought for the syllabi of the courses to be offered in the III and IV Semester of the M.A. Economics program. The syllabi conform to the DTU norms of LTP and follow the duly approved examination scheme. The contents of each syllabus were placed at Annexure pages 113 to 168 in the agenda note.

Decision : The Academic Council considered and approved the Syllabi for courses offered in the III and IV Semester, M.A. Economics.

Agenda 35.15 : Approval of seat matrices for the programs offered in East Delhi Campus.

The seat matrices for the programs- M.A. (Economics), MBA-IEV, MBA-BA, BBA-IEV, BBA and BA (H) Economics offered in East Delhi Campus were proposed by University School of Management and Entrepreneurship (USME).

Decision : The Academic Council considered and deferred the agenda for approval of seat matrices for the programs offered in East Delhi Campus. The Council, authorized Vice Chancellor to approve the seat matrices as Chairperson, Academic Council.

Agenda 35.16 : Approval of seat matrices of various undergraduate programs.

The seat matrices for various Undergraduate programs offered in Delhi Technological University were placed before the Academic Council for its consideration and approval.

Decision : The Academic Council considered and suggested to defer the agenda. The Council, authorized Vice Chancellor to approve the seat matrices as Chairperson, Academic Council.

Agenda 35.17 : Approval of revised seat matrix and approval of minor changes in eligibility criteria of MBA (Executive) admission.

Reference to Letter no. 104-86/DTU/Acad-PG/AICTE/Approval/2023-24/4300-06 dated 11/04/2023 regarding sanction intake of MBA (Executive) approved by competent authority, DTU. A committee was formed by the HOD, DSM for the deliberation on eligibility criteria and seat matrix of MBA (Executive) admission 2023-25 batch. The committee meeting was held on 12/4/2023. The committee discussed and proposed the following.

a. Since number of seats have been reduced from 75 to 60, the detailed seat matrix is prepared following the reservation of seats as per norms. The proposed seat matrix of MBA (Executive) Admission for 2023-25 batch is as follows.

Seat Matrix

Present Seat Matrix (2022-24 batch)

Category	No of Seats (intake)	PwD	Defence	Total
General (Open)	28	02	01	31
EWS	06	0	01	07
OBC	18	01	01	20
SC	10	01	0	11
ST	05	0	01	06
Total	...	...	...	75
Supernumerary seats				
Kashmiri Migrant	01	...	...	...
DTU staff	02	...	...	...

Proposed Seat Matrix (2023-25 batch)

Category	No of Seats (intake)	PwD	Defence	Total
General (Open)	22	01	01	24
EWS	05	00	01	06
OBC	15	01	00	16
SC	8	00	01	09
ST	04	01	00	05
Total	...	...	...	60
Supernumerary seats				
Kashmiri Migrant	01	...	...	...
DTU staff	02	...	...	...

b. The committee also discussed the revision of the present eligibility criteria of MBA (Executive) Admission for 2023-25 batch. The committee was of the view that the qualification criteria may be kept as it is. However, in order to provide opportunity to a wider segment of candidates, the experience criteria may be relaxed as has been implemented by some other premier Institutes such as IIT Delhi, GGSIP University. The amended eligibility criteria is as follows:

Previous eligibility criteria	Amended eligibility criteria
Graduation or its equivalent with minimum 50% marks or equivalent CGPA (10% relaxation in marks will be given to SC/ST/PwD). The student should hold a degree from any of the universities incorporated by an act of the central or state legislature in India, **or** other educational institutions established by an act of Parliament or declared to be deemed as a university under section 3 of UGC Act, 1956, **or** possess an equivalent qualification recognized by the Ministry of Education, Government of India. In case if CGPA conversion formula is not provided by the concerned Institute/University then equivalent percentage will be computed as per the DTU norms. The formula given below will be used to convert CGPA into the equivalent percentage of marks. Percentage of Marks =(CGPAx10) (For CGPA on the scale of '10') **Experience:** **Minimum 3 years work experience after four years degree (B.E., B Tech., B.Arch. etc.) .** **Minimum 4 years work experience after three years degree (B.A, B.Sc., B.Com, BCA, etc.).**	Graduation or its equivalent with minimum 50% marks or equivalent CGPA (10% relaxation in marks will be given to SC/ST/PwD). The student should hold a degree from any of the universities incorporated by an act of the central or state legislature in India, **or** other educational institutions established by an act of Parliament or declared to be deemed as a university under section 3 of UGC Act, 1956, **or** possess an equivalent qualification recognized by the Ministry of Education, Government of India. In case if CGPA conversion formula is not provided by the concerned Institute/University then equivalent percentage will be computed as per the DTU norms. The formula given below will be used to convert CGPA into the equivalent percentage of marks. Percentage of Marks =(CGPAx10) (For CGPA on the scale of '10') **Experience:** **Minimum 2 years of work experience after Under Graduate (UG) degree (B.E., B Tech., B. Arch, B.A, B.Sc., B.Com, BCA, MBBS etc.).**

Decision : The Academic Council considered and approved the revised seat matrix and minor changes in eligibility criteria of MBA (Executive) admission as above.

Agenda 35.18 : Approval of course objective for FEC courses (FEC-6, FEC-18, FEC-12, FEC-47, FEC-51) being offered to B. Tech. students.

The Delhi School of Management of the University proposed the five FECs being offered to B.Tech students. The Academic Council considered the matter and suggested some minor modifications. Accordingly, minor modifications were incorporated as under:

Revised - FEC Courses offered by Delhi School of Management

1. Subject Code: FEC-6 **Credit 2-0-0**

Course Title: Corporate Social Responsibilities

Course Objective: Gain a comprehensive understanding of CSR concepts, analyze ethical andgovernance factors in decision-making, evaluate legislative measures and their impact, and recognize the benefits of CSR for businesses and society, including social accounting and reporting.

Course Outcome:

Upon successful completion of the course the student should be able to:

1. Students will be able to explain the concepts of CSR and its approaches in the Indian andinternational context.
2. Students will be able to analyse the importance of business ethics and corporate governance, and the factors influencing ethical decision-making in different culturalcontexts.
3. Students will be able to evaluate the legislative measures related to CSR and their impacton stakeholders, labour, environment, and social accountability.
4. Students will be able to identify and discuss the benefits of CSR for businesses and society, and understand the role of social accounting, auditing, and reporting in promoting CSR.

Course Content:

1. **CORPORATE SOCIAL RESPONSIBILITIES IN INDIAN CONTEXT & INTERNATIONALCSR** - Definition, concepts, Approaches of CSR, overview of corporatesocial responsibility and corporate social accountability, SR Tools, National and InternationalCSR activities, corporate philanthropy, drivers of CSR, difference between corporate governance, corporate philanthropy and CSR
2. **BUSINESS ETHICS AND CORPORATE SOCIAL RESPONSIBILITY** - Concept of business ethics – meaning, Importance and factors influencing business ethics. Corporate Governance – meaning, significance, principles and dimensions. Ethical decision – making in different culture, consumer protection, environment protection, gender issues in multiculturalism, ethics and corruption, ethics and safety. Business benefits of CSR.

3. **LEGISLATIVE MEASURES OF CSR Corporate-** labor, stake holders, Environmental and pollution. Social Accounting, Social Auditing, SA:8000 and Corporate Social Reporting

Suggested Books:

1. The business of social responsibility, Harsh Srivastava, books for change
2. Corporate social responsibility – concepts and cases, C.V. Baxi and Ajit Prasad, Excel Books
3. Global strategic management, Dr. M. Mahmoudi, Deep & Deep Publications Pvt. Ltd.

2. Course Code: FEC -12 **Credit 2-0-0**

Course Title: Business Communication and Presentation skills

Course Objective: To understand the realistic business communication process across diverse organisations

Course outcomes:

Upon successful completion of the course the student should be able to:

1. Demonstrate proficiency in Communication skills across business settings, purposes and audiences.
2. Apply critical thinking to develop innovative and well-founded perspectives on communication globally.
3. Identify the nuances of business communication.
4. Demonstrate good business writing skills.
5. Apply the basics of nonverbal communication in professional setting.

Course Contents:

1. **IDENTITY MANAGEMENT COMMUNICATION-** Face to Face Impression Management & Mediated Communication (Self Introduction & Self Promoting– Over Stating and Under Stating – Strategies to Overcome Communicative Inhibitions – Creating Positive Self-image through words - Appearance- Verbal and Non-Verbal Manners) – Giving Polite Yet Assertive Responses – Responsive strategies to handle criticism - Accepting Failure and Declaring Success.

2. **BUSINESS PRESENTATION-** Oral and Power Point Presentations; Preparing Successful Presentations; Assessing Audience, Making Effective Use of Visual Aids, Delivering Presentation, Using Prompts, Handling with Questions and Interruptions, Mock Presentations.

3. **ORATORY SKILLS**- Group Discussion, Extempore, Mock Parliament and Mock Press.

4. **INTERVIEW MANAGEMENT**- Resume Preparation, Types of Interviews, Preparing for Interviews, Facing Interviews, Handling Tough & Tricky Questions, Reviewing Performance, Participating in Mock Interviews.

Suggested Books:

1. Business Communication, Lori Harvill Moore, Bookboon
2. Excellence in Business Communication, John Thill, Courtland L. Bovee, Pearson Prentice Hall

3. Course Code: FEC-18 **Credit 2-0-0**

Course Title: Financial Statements Analysis

Course Objectives: The objective of the financial statement analysis for any company is to provide the necessary information required by the financial statement users for informative decision making,

Course Outcomes:
Upon successful completion of the course the student should be able to:
1. To provide brief knowledge of financial statements and regulatory framework.
2. To be able to use techniques of financial statements analysis in making short-term and long-term decisions
3. To understand business drivers which derive the performance of the company.

Course Contents:
1. **INTRODUCTION TO FINANCIAL STATEMENTS**- Understanding Financial Statements-P & L, Balance Sheet, Cash Flow, Analyzing Financial Statements, interpreting Financial Statements, Ratio Analysis
2. **BUSINESS ANALYSIS-**Understanding Businesses, Overview of Key Industries, Revenue Drivers, Profitability Drivers/Cost Drivers
3. **FINANCIAL FORECASTING**- Methods of Forecasting, Balance Sheet & P& L Relationship, Understanding the Future Projections, Preparation of Forecasted Balance Sheet & Income Statement.

Suggested Books:

1. How to Read A Balance Sheet: An ILO Programmed Book, Publisher: Owford & IBH Publication Co Pvt Ltd
2. Techniques of Financial Analysis, Erich A Helfert, Jaico Publishing House.

4. Subject Code: FEC- 47 **Credit 2-0-0**

Course Title: Value Driven Leadership

Course Objectives: The objective of the value driven leadership is to develop the understanding of values , concepts workforce diversity, innovation, ethical and legal regulatory frameworks, unethical behaviour, truth, marketing practices, incentives in businesses and solutions, different approaches for solutions in organisational context and to develop the importance of social and intellectual capital to create value.

Course Outcomes:

Upon successful completion of the course the student should be able to:

1. To understand foundational concepts of morals, ethics, values, integrity, justice, fairness, character, civility, and community, conflicts and their relevance in different contexts.
2. Assess the role of corporate social responsibility (CSR), Companies Act, value-based marketing, ethical implications and work force diversity in businesses.
3. Analyze the impact of social and intellectual capital and approaches for solutions.
4. Apply the knowledge for solutions to organization practical and specific problems.

Course Content

1. **Introduction and Resolving Conflicts of Values within and between other Stakeholders:** Introduction to Concepts like Morals, Values, Ethics, Trust. Integrity Justice Fairness, Character, Civility and Community, Conflicts, Stakeholders. Issues of Conflicts. Resolving Conflicts of Values within and between other Stakeholders Workforce Diversity and Corporate Social Responsibility
2. **Workforce Diversity and Corporate Social Responsibility:** Diversity, Types of Diversity, Benefits of Workforce Diversity. Corporate Social Responsibility. Milton Friedman's Approach, Companies Act and Corporate Social Responsibility
3. **Managing Values through Incentives and Informal Mechanisms:** Managing Values, Incentives, Material Incentives, Informal Mechanisms, Managing Values through Incentives and Informal Mechanisms
4. **Speaking the Truth and Values Based Marketing:** Truth, Unethical Behaviour, Situations where Truth is dangerous for the organization, Importance of Speaking the Truth. Ethical implications of Marketing Values Importance of Values Based Marketing. Thomas Donaldson's Ethical Algorithm.

5. **Building Social Capital:** Social Capital, Constituents of Social Capital, Importance of Social Capital for an) Organization, Use Organizational Intellectual Capital to Create Value

Suggested Books:

1. Values-Driven Leadership by Peter Evans, Doug Hargreaves. Tilde University Press, ISBN-13:9780734610867
2. From Values to Action: The Four Principles of Values-Based Leadership Jossey-Bass; I edition, John Wiley
3. The Power of Character in Leadership: How Values, Morals, Ethics, and Principles Affect Leaders, Whitaker House. Alternate edition

5. Subject Code: FEC-51 **Credit 2-0-0**

Course Title: Entrepreneurship exploration

Course objectives: The objective of this course is to create awareness about entrepreneurship among students and help them imbibe an entrepreneurial mindset.

Course Outcomes:

Upon successful completion of the course the student should be able to:

1. Develop an entrepreneurial mind-set by learning key skills.
2. Identify real life business problems and transform them into sustainable business opportunities.
3. Create and validate a business plan and pitch it to all stakeholders.
4. Understand the basics of organization and team building.

Course Content:

The course has been designed as a practical course and therefore no regular classes will be conducted. However, few classes will be conducted on following topics: starting small business, planning, organizing, and managing human resources. Additionally, few motivational lectures in the form of success stories will be conducted for the students.

A group of maximum two (02) students who registers for this course will be given an initial seed money upto Rs 10,000/- to start a small business. This will help students in realizing their entrepreneurship potential. The students will submit a business plan in the 1st Week of commencement of academic session. A group of maximum two (02) students can register for this elective at the beginning of I-III semester. The registered team should conceptualize a business idea and will submit a proposal in the Dean (UG) office DTU-IIF within 1st Week of commencement of semester registration.

A Mentor Committee, comprising of :-

(i) Chairperson(s)
(ii) A Faculty Member / Course Coordinator and
(iii) External Expert will approve/ reject proposals based on merits and expected outcome of the proposal.

The same committee may also assign the maximum possible grades for the course. The students will submit a detailed project report at the end of semester for evaluation.

The university will not be responsible for loss beyond the seed money. However, the profit will be divided proportionally.

Suggested Books:

Small Business Management- An Entrepreneur's Guidebook by Byrd Megginson, McGraw-Hill, Irwin. ISBN 978-0-07-802909-7.

Decision : The Academic Council considered and approved the course objective for FEC courses (FEC-6, FEC-18, FEC-12, FEC-47, FEC-51) being offered to B. Tech. students as modified above.

Agenda 35.19 : Matter for ratification.

i. **Admission Brochure for International Students for AY 2023-24.**

It was submitted to the Academic Council that the Admission Brochure for International Students for academic year 2023-24 of the University has been approved by the Competent Authority after incorporating the necessary changes. The brochure was tabled for ratification of the Academic Council.

ii. **Changes made in Eligibility criteria for UG & PG programs for International students.**

It was submitted to the Academic Council that Chairperson, Academic Council has revised the eligibility criteria for UG & PG programs for International students is as under:

For Undergraduate Programs-

Applicant should have 60% aggregate marks or 6.00 CGPA on a 10 point grade or equivalent grades for B.Tech students, **60 % marks or 6.00** CGPA on 10 point grade or equivalent grades for **BBA, B.A (Economics) and B.DES** students in aggregate for all subjects of qualifying examination i.e Senior Secondary [10+2] orequivalent from any system of education as recognized by the Association of Indian Universities (AIU) with:

a) Physics and Mathematics as compulsory subjects and any one of the following subjects Chemistry,Bio-technology, Computer Science, Biology foradmission to B.Tech program.
b) Mathematics as one of the compulsory subject foradmission to BA (H) Economics.
c) English as a compulsory subject for admission to BBA program.
d) Any stream of courses for B.DES program

For Postgraduate Programs-

For MBA program: An appropriate UG degree from any stream of education **along with valid CAT/MAT score**.

iii. **Admission Brochure for 05 Post-Graduate and Ph.D programs for the academic year 2023-24.**

It was submitted to the Academic Council that the Admission Brochure for 05 Post-Graduate i.e *MBA, MBA(BA), MBA (Executive), M.Sc., M.Tech. and Ph.D programs for academic year 2023-24* of the University has been approved by the Competent Authority after incorporating the necessary changes. The brochure is tabled for ratification of the Academic Council.

iv. Annual Quality Assurance Report, 2021-22.

It was submitted to the Academic Council that as per mandate of National Assessment and Accreditation Council (NAAC), the University data in the form of 'Annual Quality Assurance Report (AQAR)' is to be complied and uploaded on NAAC website after the approval of the Statutory body of the University.

Accordingly, the AQAR of the University for the year 2021-22 was prepared and has been uploaded on NAAC website after approval of the Vice Chancellor in capacity of Chairman, Academic Council. The approved AQAR was placed in agenda note at Annexure pages 169 to 279.

v. Name change of M.Tech programme in Department of Information Technology - M.Tech (Information Systems) to M.Tech (Information Technology).

A proposal was received from the HOD(IT) towards change of Branch Name Master of Technology in Information Systems(ISY) to Master of Technology in Information Technology(IT). According to him, many of M.Tech. (ISY) 1st year students have submitted applications in the Deptt. of Information Technology requesting therein to change M.Tech. Programme name from Information System(ISY) to Information Technology (IT) with the following reasons given below:

(i) ISY programme may not be well known among recruiters and some of companies do not shortlist the students of ISY for campus placements.

(ii) Most of the Institutes of national importance like IIT & NIT's which similar course structure like ours have M.Tech. programme name as M.Tech. in Information Technology (IT).

(iii) Current name as "M.Tech. in ISY" does not accurately reflect the fours of our program and may be less attractive to potential recruiters. By changing the name of branch name from M.Tech. (ISY) to M.Tech. (IT) would be better able to communicate the true nature of program to all recruiters of students.

The BOS of the IT Department has also unanimously recommends the change of branch name from M.Tech. in Information Systems (ISY) to **M.Tech. in Information Technology (IT)**.

It was pertinent to mention here that as per approval of the Hon'ble VC as Chairperson of Academic Council, name change has already been applied as M.Tech. (Information Technology) in the application of AICTE Approval Process 2023-24.

vi. Closure of 01 MBA (FBE) course for the Academic year 2023-24.

A proposal was received from the HOD(USME) towards AICTE approval for MBA (FBE) course may not be sought and "closure of course" for the Academic Year 2023-24 due to following reasons:

Number of admission in MBA (FBE) course in last three consecutive years were very less and no admission in year 2022. The details of the admission of last 03 years are as under:

Program	Sanctioned Intake (DTU)	AICTE approved intake	Admitted Student in last 03 years
MBA (FBE)	40	30	2020-21: 8 2021-22: 15 2022-23: Nil

The BOS of the Department of USME has also recommends the AICTE approval for FBE may not be sought and "closure of course" for the Academic Year 2023-24.

It was mentioned that as per approval of the Hon'ble VC as Chairperson of Academic Council, renewal of approval for MBA (FBE) not applied in the application of AICTE Approval Process 2023-24.

vii. Minor Change in Criteria for Part Time Ph.D. Admissions for the Academic Year 2023-24.

The following changes were proposed by the admission committee for inclusion in Admission Brochure for the upcoming Ph.D. Admissions for the Academic Year 2023-24 for Part-Time category:

Category	Previous	Revised
Part- Time Research student/candidate	Faculty or scientists from Educational Institutions, R&D organizations, and Government Department/Public Sector Undertaking/Candidates from industry of high repute and a medium sized enterprise with turnover Rs. 75 crores or above along with standing commitment to the exemplary standards namely ISO/CMM level 3 or similar standard of respective area provided that the applicant possesses the minimum eligibility qualifications for the degree.	**Candidate employed in** Educational Institutions/ Universities, R&D organizations, and Government Department, Public Sector Undertaking and Candidates from active industry/companies of high repute and a medium sized enterprise along with standing commitment to the exemplary standards namely ISO/CMM or similar standard of respective area provided that the applicant possesses the minimum eligibility qualifications for the degree.

It was mention that after approval of the Hon'ble Vice Chancellor as Chairperson of Academic Council, proposed minor changes in criteria for Ph.D. Part Time Category have been incorporated in Admission process/brochure for the Academic Year 2023-24.

viii. Minor Change in Criteria for Full Time Sponsored M. Tech. Admissions for Academic Year 2023-24.

The following changes were proposed by the admission committee for inclusion in the Admission Brochure for the upcoming Ph.D. Admissions for the Academic Year 2023-24 for Full Time Sponsored category:

Category	Previous	Revised
Full- Time Sponsored candidate	Faculty or scientists from Educational Institutions, R&D organizations, and Government Department/Public Sector Undertaking/Candidates from industry of high repute and a medium sized enterprise with turnover Rs. 75 crores or above along with standing commitment to the exemplary standards namely ISO/CMM level 3 or similar standard of respective area provided that the applicant possesses the minimum eligibility qualifications for the degree.	**Candidate employed in** Educational Institutions/ Universities, R&D organizations, and Government Department, Public Sector Undertaking and Candidates from active industry/companies of high repute and a medium sized enterprise along with standing commitment to the exemplary standards namely ISO/CMM or similar standard of respective area provided that the applicant possesses the minimum eligibility qualifications for the degree.

It was mentioned that after approval of the Hon'ble Vice Chancellor as Chairperson of Academic Council, proposed minor changes in criteria for M.Tech. Full Time Sponsored Category have been incorporated in Admission process/brochure for the Academic Year 2023-24.

ix. Minor Changes in Criteria for Industry/Working Professionals in Ph.D. Programme for the Academic Year 2023-24.

The following changes were proposed by the admission committee for inclusion in Admission Brochure for the upcoming Ph.D. Admissions for the Academic Year 2023-24 for Industry/Working Professional category:

Category	Previous	Revised
Industry Working Professional (IWP)	Eligibility Criteria 2. Bachelor's degree in Engineering/ Technology/ Sciences/Management / Humanities and Social Sciences in relevant discipline or equivalent degree with: a) More than 05 years and less than 10 years work experience* CGPA of 7.0 on a 10-point scale or 70% marks **'OR'** b) More than 10 years and less than 15 years work experience* CGPA of 6.5 on a 10-point scale or 65% marks	Eligibility Criteria 1. Bachelor's/Master's Degree in Engineering/ Technology in relevant discipline or equivalent** degree with: a) More than 05 years and less than 10 years work experience* CGPA of 7.0 on a 10-point scale or 70% marks **'OR'** b) More than 10 years and less than 15 years work experience* CGPA of 6.5 on a 10-point scale or 65% marks

	'OR' c) more than 15 years work experience* CGPA of 6.0 on a 10-point scale or 60 % marks 3. Credentials of the company/ organization of the working professional applying for the program shall be assessed on the basis of following mandatory criteria: a) The reputation of the companies (private or government or PSU's), Research Organizations, Ministries of Central and State Governments or Union Territories or Recognized Research Institutes or Public Sector Undertaking or Semi-Govt. or Autonomous or Statutory organisations/ institutions or Registered Companies or industrial research and development organisations excluding academic institutions. b) **Annual turnover of at least rupees 50 crore or above with standing commitment to the exemplary standard namely, ISO, CMM level 3 or similar standard of respective areas mandatory for any enterprise / company / industry / firm.** c) The candidate must have the working experience at least continuous 02 years in the respective organization/institution at the time of application along with the work experience indicated in Point (1) above. d) A research proposal approved by the prospective supervisor must be submitted by the candidate at the time of the application.	**'OR'** c) more than 15 years work experience* CGPA of 6.0 on a 10-point scale or 60 % marks 2.Credentials of the company/organization of the working professional applying for the program shall be assessed on the basis of following mandatory criteria: a) The reputation of the companies (private or government or PSU's), Research Organizations, Ministries of Central and State Governments or Union Territories or Recognized Research Institutes or Public Sector Undertaking or Semi-Govt. or Autonomous or Statutory organisations/ institutions or Registered Companies or industrial research and development organisations excluding academic institutions b) **With standing commitment to the exemplary standard namely, ISO/CMM or similar standard of respective areas mandatory for any enterprise / company / industry / firm.** c) The candidate must have the working experience at least continuous 02 years in the respective organization/ institution at the time of application along with the work experience indicated in Point (1) above. d) A research proposal approved by the prospective supervisor must be submitted by the candidate at the time of the application.
	**Work experience may include position in multiple organization(s), such candidate shall be working on industry oriented research problems.*	**Work experience may include position in multiple organization(s), such candidate shall be working on industry oriented research problems.*

	** *Equivalence of degree will be decided by the University.*	** *Equivalence of degree will be decided by the University.* *** *For candidate applying with higher degree under this category of IWP, the eligibility as per point no. 5 Admission Eligibility of Admission Brochure.*

It was mentioned that after approval of the Hon'ble Vice Chancellor as Chairperson of Academic Council, minor changes in criteria for Ph.D. Industry/Working Professional Category have been incorporated in Admission process/brochure for the Academic Year 2023-24.

x. **Ratification towards proposal of registration in 3rd Semester in M.Tech Program in r/o Mr. Shashank Khare (2K18/ENE/09).**

Mr. Shashank Khare has completed M.Tech. (ENE) 1st Year with 8.05(1stSem) & 8.10 (2ndSem SGPA (Page- 26 & 27/C) and has earned 40 credits in the Old Scheme. He has now requested to complete his M.Tech. degree. The DTU have adopted New Scheme in M.Tech. Programme since 2019 and he may be allowed to register in 3rd Semester and complete his degree in New Scheme.

3rd Semester New Scheme			
Elective Subjects	**Credits**	**Remarks**	**Revised Mode**
S.No. 07 – ENE-6401 - Environmental Impact Assessment and Audit (Flagged at 'A')	04	In the 3rd Semester New Scheme, there are three Elective papers at S.No. 07, 08, 09 which are similar to the Elective Subjects available in the Old Scheme (Flagged at 'B').	Proposed to complete credits in New Scheme with online MOOC courses through Swayam, NPTEL etc. platforms duly approved by the BOS of the concerned Department to ascertain the relevance of subject.
S.No. 08- ENE-6301 Air Quality Modeling (Flagged at 'A)	03		
S.No. 09 – ENE6201 - Hazardous Waste Management (Flagged at 'A)	02		
Major Project-I	03		The evaluation will be done at the department level
4th SemesterNew Scheme			
Major Project-II	12		The evaluation will be done at the department level
Total Credits required to complete Degree	**58**	Credits Earned by Mr. Khare: **66** (42 old scheme + 24 new Scheme)	

Further, it was submitted that Mr. Shashank is working in Satluj Jal Vidyut Nigam, Public Section Undertaking under the Government of Himachal Pradesh and is presently posted at Shimla and it will not be possible for him to attend classes regularly.

After considering the all the facts of the case, Hon'ble Vice-Chancellor as the Chairman, Academic Council has permitted Mr. Shashank Khare to complete M.Tech. degree in New Scheme and to opt for the elective courses through online MOOC: NPTEL, Swayam etc. platforms. It was mentioned that the Board of Studies of the Department will approved the equivalence of the ONLINE courses.

Decision : The Academic Council ratified the above actions of the University.

Agenda 35.20 : Matter for information.

i. Admissions made in Ph.D. program for the winter session January 2023.

Sixty seven admissions were made in Ph.D program for the winter session January 2023. The list of the 67 admitted students for the said program was placed in agenda note at Annexure pages 280 to 282.

ii. Formal registration to Ph.D. students upon successful completion of course work and comprehensive examinations and approval of research Plan by respective DRCs.

One hundred students have been registered in Ph.D. program upon successful completion of course work and comprehensive examinations and approval of research Plan by respective DRCs. Department-wise list of the registered Ph.D. students was placed in agenda note at Annexure page 283 to 288.

iii. Cancellation/Withdrawal of admission from Ph.D program.

It was submitted to the Academic Council that following 12 candidates have withdrawn their admission from Ph.D. program:

S. No.	Roll No.	Full Name	Department	w.e.f.
1.	2K19/PHDAM/08	DhruvGoel	Applied Mathematics	22.09.2022
2.	2K18/PHDEN/05	Sugandh Singh	Environment Engineering	22.07.2022
3.	2K19/PHDEN/502	MotiualHaq Ansari	Environment Engineering	22.07.2022
4.	2K15/PHDEN/01	Lokesh Kumar	Environment Engineering	22.07.2022
5.	2K19/PHDCE/12	Manoj Kumar	Mechanical Engineering	26.10.2022
6.	2K17/PhD/ME/30	Arvind Kumar	Mechanical Engineering	26.10.2022
7.	2K11/PHDEE/02	Arshad Husain Quadri	Electrical Engineering	18.11.2022
8.	2K17/PHDEE/17	Ritesh Kumar Sharma	Electrical Engineering	18.11.2022
9.	2K18/PHDEE/19	SumitMaheshwari	Electrical Engineering	18.11.2022
10.	2K18/PHDUSME/02	Shilpika Gera	USME	17.11.2022
11.	2K21/PHD/IT/10	Manish Kumar	Information Technology	11.01.2023
12.	2K19/PhD/CO/1	Piyush Khandelwal	Computer Science and Engineering	29.10.2022

Agenda 35.21 : Any other item with the permission of the Chair.

Supplementary Agenda 35.22 : Proposed changes in the admission criteria for admission in Ph.D (Geoinformatics) under department of Civil Engineering.

It was submitted that **Multidisciplinary Centre for Geo-informatics (MCG) is functioning under the Department of Civil Engineering.** Due to multidisciplinary nature of the Geoinformatics subject, certain issues were observed in the Ph.D Admission criteria as reflected in the Ph.D Admission Brochure. The present agenda item sought to address/correct these issues.

This issue was deliberated under Agenda Item No 32.17 in the 32nd AC Meeting under the title, 'Minor modifications in Ph.D Admission Criteria for the Department of Civil Engineering'. The Academic Council deliberated but deferred the matter and constituted a Committee under the Chairmanship of Prof. Nirendra Dev with Prof. S. Indu, Prof. V.K. Minocha, Sh. Rajesh Mathur and Prof. K.C. Tiwari as members to look into the issue in detail.

The Committee after deliberations recommended the following for consideration of the Academic Council -

(i) **Introduce 'Geoinformatics' as a separate discipline** under the Multidisciplinary Centre for Geoinformatics in the Department of Civil Engineering.

(ii) The **eligibility criteria for admission in Ph.D in Geoinformatics** be brought at par with the M.Tech (Geoinformatics) admission eligibility which is as under –

Academic Department	Discipline Offered	Qualifying Degree
Civil Engineering	Geoinform -atics	Master's degree in Engineering / Technology or equivalent in any branch/discipline with a minimum 55% marks in aggregate or equivalent CGPA as determined by DTU **OR** Master's degree in Computer Applications/Sciences/Arts or equivalent in any branch/discipline with a minimum 55% marks in aggregate or equivalent CGPA as determined by DTU **OR** Bachelor's degree in Engineering / Technology in relevant discipline or equivalent with a minimum 75% marks in

		aggregate or equivalent CGPA and having proven research capability. **NOTE – The students will be supervised by faculty from relevant departments with vacancy slots**

(iii) Till the Centre (Multidisciplinary Centre for Geoinformatics) continues to be in the Department of Civil Engineering, the Ph.D Degree should read – ".....Mr. XXX registered in the ***Department of Civil Engineering*** is awarded degree of Doctor of Philosophy in the Discipline of ***Geoinformatics***".

(iv) The advertisement as well as the Ph.D Admission brochure should clearly highlight multidisciplinary/interdisciplinary Subjects/Centers as done by various premier institutes.

(v) The Centre should draw its faculty not only from Civil Engineering Department but interested faculty from all the Departments for the purpose of supervising/guiding Ph.D in any Geo-informatics area. The Ph.D slots will be determined based on the interested faculty. The SRC/DRC may also be redrawn from the faculty associated with the Centre.

Decision : The Academic Council discussed that Multidisciplinary Centre for Geoinformatics is currently under the Department of Civil Engineering. Students from other departments joining the Centre are awarded degree of the Department of Civil Engineering. It often causes hardships to the students while seeking employment. The Academic Council, therefore, approved for making the Centre independent with immediate effect.

Supplementary Agenda 35.23 : Proposed changes in the admission criteria for admission in M.Tech (Geoinformatics) under Department of Civil Engineering.

It was submitted to the Academic Council that **Multidisciplinary Centre for Geo-informatics (MCG) is functioning under the Department of Civil Engineering.** Due to multidisciplinary nature of the Geoinformatics subject, certain issues were observed in the M.Tech Admission brochure. The present agenda item sought to address/correct these issues.

Currently, the eligibility conditions for M.Tech (Geoinformatics) in the M.Tech Admission Brochure has the following information -

Department/ Program Name	Qualifying GATE Subject	Qualifying Degree
Civil Engineering		
Geoinformatics	CE	BE / B. Tech / MCA / M. Sc in Civil / Architecture/ Agriculture / Geomatics/ Geoinformatics/ Geography/ Computer Science and Engineering/ Information Technology/ Software Engineering/ Electronics and Communication Engineering/ Electrical Engineering/ Mathematics/ Physics/ Geology disciplines and equivalent.

Following deficiencies were observed –

(a) Although the qualifying degree for M.Tech (Geoinformatics) lists out several degrees/streams, the qualifying GATE subject mentioned is only CE (Civil Engineering). This in essence means that a B.Tech (CSE/IT/ECE) student though eligible has to qualify GATE Exam in Civil Engineering only if he wants to take admission in Geo-informatics. This restriction does not make the subject of Geoinformatics multidisciplinary and is a huge demotivation for the students interested in pursuing this subject.

(b) It was also observed that the list of Qualifying Degrees **does not include – 'Environmental Engineering'**. Last year, a few DTU students from Environment Department were denied admission in M.Tech (Geoinformatics).

(c) It was also submitted that **GATE Exam now has a subject 'Geomatics' w.e.f. 2022** and a large number of students have qualified GATE (Geomatics) 2022. This year onwards students with GATE (Geomatics) score are also likely to apply for admission.

In view, the following amendments were recommended –

(a) Amendments in the Admission Criteria to be inserted in the M.Tech Admission Brochure -

Program Name	Qualifying GATE Subject	Qualifying Degree
Civil Engineering		
Geoinformatics	Aerospace Engineering, Agricultural Engineering, Architecture and Planning, Civil Engineering, Computer Science and Information Technology, Electronics and Communication Engineering, Electrical Engineering, Environmental Science & Engineering, Ecology and Evolution, Geomatics Engineering, Geology and Geophysics, Instrumentation Engineering, Mathematics, Mechanical Engineering, Mining Engineering, Naval Architecture and Marine Engineering, Petroleum Engineering, Physics, Statistics, Engineering Sciences,	(aa) BE/ B.Tech/ B.Arch/ B. Planning or equivalent in any branch of Engineering and Technology (ab)M.Sc in Agriculture /Remote Sensing / GIS /Geomatics/Geo-informatics/Geography / Environment Science /Mathematics/Physics/ Geology/Disaster-Management/Sustainable Development (ac) MCA or equivalent

(b) The total number of seats (out of 18) should be distributed as follows. 11 seats for Qualifying Degree category (aa) i.e B.E/B.Tech/ B.Arch/ B.Planning, 4 seats for Qualifying Degree category (ab) i.e M.Sc. and 3 seats for Qualifying Degree category (ac) i.e MCA or equivalent. During the spot round, all seats will be merged and offered in the priority, first - Qualifying Degree category (aa) i.e BE/B.Tech/B.Arch/B.Planning, second, Qualifying Degree category (ab) i.e M.Sc. and third, Qualifying Degree category (ac) i.e MCA students.

(c) ***A common merit of GATE score be made for shortlisting.***

Decision : The Academic Council considered and approved the proposed changes in the eligibility criteria for admission in M.Tech (Geoinformatics) and its implementation under an independent Multidisciplinary Centre for Geoinformatics.

The meeting ended with vote of thanks to the Chair.

(Prof. Madhusudan Singh)
Registrar

No. F.DTU/Council/AC/Meeting/51/2022/744 Date : 12/6/2023

Copy to:-

1. Secretary to Hon'ble Lt. Governor (Delhi), 6, Raj Niwas, Civil Lines, Delhi.
2. Vice Chancellor, DTU
3. Prof. J.P. Saini, Vice Chancellor, Netaji Subhash University of Technology, Dwarka, Delhi (UGC Nominee)
4. Prof. Neharika Vohra, Former Vice Chancellor, Delhi Skill & Entrepreneurship University, Dwarka, Delhi.
5. Prof. D.P. Goyal, Director, Indian Institute of Management, Shillong, Meghalaya
6. Prof. Bhim Singh, Professor, Indian Institute of Technology, Delhi
7. Dr. B.R. Chahar, Professor, Indian Institute of Technology, Delhi (AICTE Nominee)
8. Sh. Rajesh Mathur, Advisor, ESRI, 5142, Laurel Parks Laureate, Sector 108, Noida 201304, Uttar Pradesh
9. All Deans of the University
10. Prof. Reeta Wattal, Professor, Mechanical Engineering
11. Prof. V.K. Minocha, Professor, Civil Engineering
12. Prof. Pragati Kumar, Professor, Electrical Engineering
13. All Heads of the Schools/Departments, DTU
14. Controller of Examinations, DTU
15. Sh. Rajesh Birok, Associate Professor, Electronics and Communication Engineering
16. Dr. M. Jayasimhadri, Assistant Professor, Applied Physics
17. Registrar

(Prof. Madhusudan Singh)
Registrar

ANNEXURE
for
Minutes

35th meeting of
Academic Council
DTU

15-05-2023

Shahbad Daulatpur, Bawana Road, Delhi-110042

Annexure 35.9

Proposal

for

Establishment of

Vinod Dham Centre of Excellence for Semiconductors and Microelectronics

(VD CoE4SM)

Delhi Technological University

May 2023

Contact Person:

1. Prof. Rishu Chaujar,
Coordinator, VD CoE4SM
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TITLE: Vinod Dham Centre of Excellence for Semiconductor and Microelectronics (VDCoE4SM)

TITLE: Vinod Dham Centre of Excellence for Semiconductor and Microelectronics (VDCoE4SM)

1. INTRODUCTION

As the world continues to reel from a dearth of semiconductors, it has become extremely vital to secure supply chains from geopolitical risks and natural disasters. While the Covid-19 pandemic may have exacerbated the demand-supply imbalance in chips, the signs of an impending crisis had appeared long before the pandemic. Apart from negative variables like the U.S.-China trade war, the concentration of advanced manufacturing capabilities in the hands of a few players had significantly constricted the entire value chain. To build resilience in the future, it will be important to identify and mitigate potential disruptions to the semiconductor industry. More broadly, there is a pressing need to look beyond microchips and anticipate threat factors for the electronics industry and other allied sectors. Hence, Delhi Technological University has established a Vinod Dham Centre of Excellence for Semiconductors and Microelectronics in order to support Government of India's vision to build a vibrant Semiconductor and Display Ecosystem enabling India's emergence as a global hub for electronics manufacturing and design. The Centre will help in developing a semiconductor and display eco-system for transformation from a wafer to chips to start-ups. State-of-the-art facility for training, fabrication & testing will be created to carry out interdisciplinary research in Semiconductor technologies, Microelectronics and associated areas. The Centre has been established to impart training & research in thrust area of Semiconductor Technology and IC Manufacturing; and also provide a platform to boost productivity, address emerging skill gaps and align training & research with industry needs.

This Centre will not only provide interdisciplinary research and development ecosystems but also offer internships, skills development courses, entrepreneurship programs and will facilitate industrial trainings for undergraduate/postgraduate students and research scholars for skilling, reskilling, and upskilling considering the existing capacity and skill ecosystem in the country.

In addition, the Centre will also offer regular PG/certificate courses in the near future. The facility will strive for networking and collaboration with industries, research laboratories, and other institutions of excellence in India and abroad to carry out cutting-edge research and development in Semiconductor Technologies and Microelectronics, along with offering certificate/postgraduate programmes.

Many faculty members of the different departments are already working in different areas related to Semiconductor Technology and Microelectronics through various sponsored research projects. These islands of research endeavours and the

expertise of the faculty members involved in the team can be gainfully collaborated for the conceptualization and development of this Centre of Excellence. However, sustaining the operations of the Centre of Excellence and its various activities including interdisciplinary research and development, internships, skill development, entrepreneurship program and facilitating industrial training for undergraduate/postgraduate/doctoral programs along with collaboration with industries and leading university academic institutions of excellence will require additional faculty members along with associated technical and administrative staff and provision of budgetary support.

1.1. VISION OF THE CENTRE

To stimulate and create a robust R & D ecosystem that drives innovation, IP and start-ups in Semiconductor Technology and Microelectronics to cater to the Nation's scientific demands; and serve as a Centre of National and Strategic importance.

1.2. MISSION OF THE CENTRE

1. To be a trusted technology and capacity provider of the global Semiconductor and Microelectronics industry with a sustainable impact through innovative semiconductor technologies and solutions.

2. To create environment of research, collaboration, innovation and skill development bridging the gap between academia and industry.

3. To provide ethics and value-based education by promoting activities addressing the societal needs.

4. To enable students develop skills to solve complex technological problems of current times and create world class professionals competent enough in the area of Semiconductors and Microelectronics.

1.3. OBJECTIVES:

1. To establish a centralized state of the art infrastructure facility for next generation device design/materials research/fabrication and sustain educational resources for cutting edge Research and Development in Semiconductor and Microelectronics.

2. Capacity building in terms of skilled manpower at different levels such as technicians, supervisors and engineers in the area of Semiconductor Technology, IC Manufacturing and Microelectronics.

3. Design the curriculum with desired skill sets in research, design, fabrication, equipment manufacturing, packaging, and other related fields for development of Indian semiconductor and display ecosystem.

4. To offer internship opportunities to the students of degree, diploma and certificate level institutions at state and national levels under Govt of NCT of Delhi.

5. To offer M.Tech and Ph.D. programmes in the area of Semiconductors, IC Manufacturing and Microelectronics.

6. Collaboration between Delhi Technological University and Semiconductors/Microelectronics Industry in order to align training & research as per industry needs.

1.4. TIMELINE

The establishment of VDCoE4SM would be done in a phased manner as given under:

- **Phase I: (First 12 months)**

1. **Creation of infrastructure for VDCoE4SM :**
   The Centre is being envisioned as an independent centre and we will require dedicated space, equipment and manpower. The University has sufficient space available for the establishment of this Centre. A separate building will be provided in the university for VDCoE4SM. The Centre will have different laboratories and as such equipment required there will be procured from the grants received from different funding agencies. Additionally, faculty positions, technical and supervisory staff position will be created for the Centre, pending which some faculty and staff positions may be transferred from the different departments of the university. The University may have joint faculty positions in the Centre with various other departments.

2. **Consolidation of Areas of Research :**
   Consolidation of islands of research in the different areas related to Semiconductors and Microelectronics through various Sponsored Research Projects undertaken by the faculty members of Department of Applied Physics, DTU and identification of niche areas of interdisciplinary research in Semiconductors, IC Manufacturing, Microelectronics and its associated areas.

3. **Procurement of Electronic Design Tools/Software/Equipment:**
   The detailed specifications of various tools and equipment will be finalized after carrying out a detailed study of existing semiconductor technology and development facilities and discussions with OEM and suppliers dealing with the

IC manufacturing and chip designing. The tendering and procurement of the equipment will start during the next phase.

- **Phase II: (Next 12 months)**

1. **Procurement of Electronic Design Tools/Software/Equipment:**
   The procurement initiated in Phase-I will be completed in this phase. Further, the Centre will initiate collaboration with different industry partners in the area of Semiconductors, IC Manufacturing and Microelectronics.

2. **Training and Courses:**
   After creation of the required infrastructure, the Centre will start training and student internship programmes for different levels of manpower such as design engineers, process engineers and technicians in the areas related to maintenance, repair and manufacturing.

3. **Course Development:**
   The Centre will also start Postgraduate and Ph.D programs related to Semiconductors and Microelectronics after taking approval from different regulatory bodies. Also, to promote research and development activities in the frontier areas of Semiconductor and IC manufacturing, the University will create full time Ph.D. research fellowships for the Centre.

1.5. INFRASTRUCTURE

Delhi Technological University has adequate space for establishment of a Centre of Excellence for Semiconductors and Microelectronics. The Centre will start in a separate space as marked for the Centre. The Centre will have different laboratories and as such, the tools, softwares and equipment required therein, will be procured from the grants received from different funding agencies.

2. DETAILED PROJECT PROPOSAL

2.1. BACKGROUND

Ministry of Electronics and Information Technology has come out with National Policy on Electronics 2019 (NPE-2019) with a vision to position India as a global hub for Electronics System Design and Manufacturing (ESDM) by encouraging and driving capabilities in the country for developing core components, including chipsets, and creating an enabling environment for the Industry to compete globally. One of the objectives of National Policy of Electronics is to promote domestic manufacturing including core components and materials and to reduce dependence on import of electronic goods by focusing on skill, technology, scale and the global market with a target to achieve the turnover of USD 400 billion (approximately INR

26,00,000 crore) by 2025.To achieve this target, some of the strategies identified in NPE 2019 are to (i) encourage participation of academic institutes in smaller cities in addition to premier institutes, (ii) bring collaborative R&D between academia and industry iii) Provide support to start-ups in emerging areas/ technologies from supporting the concept to development/ prototyping of products, including the complete value chain (iv) Set up a framework for creation of an ecosystem for promoting design of IPs in the country. Thus, the National Policy of Electronics not only aims to provide support for significantly enhancing the availability of skilled manpower to the industry but also to encourage the industry led R&D and innovation in all sub-sectors of electronics by promoting path-breaking research, grass root level innovations and early-stage Start-ups in emerging technology Projects. In line with the objective and vision of NPE-2019, an umbrella programme "Chips to Startup (C2S)" Programme has been proposed which not only aims at developing Specialized Manpower in VLSI/Embedded System Design domain but also addresses each entity of the Electronics value chain via Specialized Manpower training, Creation of reusable IPs repository, Design of application-oriented Systems/ASICs/FPGAs and deployment by academia/ R&D organization by way of leveraging the expertise available at Startups/MSMEs.

Expediting the next and future generations of semiconductor systems will impact all aspects of modern life and all industries of our economy. The future of semiconductor manufacturing will require the design and deployment of diverse new technologies in materials, chemical and materials processes, devices, architectures through the development of application-driven systems, and engaging the full spectrum of talent in the academic community and industrial sectors. Partnerships between industry and institutions of higher education are essential to spur innovation and technology transfer, to inform the research needs, and to educate future researchers and train the future workforce.

2.2. NEED FOR PROMOTING THE SEMICONDUCTOR MANUFACTURING AND CHIP DESIGN

The vision of Government of India's Semiconductor Mission is to build a vibrant semiconductor and display design and innovation ecosystem to enable India's emergence as a global hub for electronics manufacturing and design in a more structured, focused, and comprehensive manner through various mechanisms. India is aiming to become the global hub for semiconductor design, manufacturing and technology development. However, the shortage of semiconductor chips has exposed vulnerabilities in the semiconductor supply chain and highlighted the need for increasing domestic manufacturing capacity. Moreover,

- Semiconductor chips are the lifeblood of the modern information age. They enable electronic products to compute and control actions that simplify our lives.

- These semiconductor chips are the drivers for ICT (Information and Communication Technologies) development and one of the key reasons for the current flattening of the world.
- They are used in critical infrastructures such as communication, power transmission, etc., that have implications for national security.
- Development of the semiconductor and display ecosystem will have a multiplier effect across different sectors of the economy with deeper integration to the global value chain.

2.3 INDIA'S POSITION IN SEMICONDUCTOR MARKET

India currently imports all chips and the market is estimated to touch $100 billion by 2025 from $24 billion now. However, for the domestic manufacturing of semiconductor chips, India has recently launched several initiatives:

- The Union Cabinet has allocated an amount of ₹76,000 crore for supporting the development of a 'semiconductors and display manufacturing ecosystem'.
- Consequently, a significant amount of incentives would be provided to design companies to design chips.
- India has also launched the Scheme for Promotion of Manufacturing of Electronic Components and Semiconductors (SPECS) for manufacturing of electronics components and semiconductors.
- In 2021, the MeitY also launched the Design Linked Incentive (DLI) Scheme to nurture at least 20 domestic companies involved in semiconductor design and facilitate them to achieve a turnover of more than Rs.1500 Crore in the next 5 years.
- India's own consumption of semiconductors is expected to cross USD 80 billion by 2026 and to USD 110 billion by 2030.

2.4 CHALLENGES FACED

- High Investments Required: Semiconductors and display manufacturing is a very complex and technology-intensive sector involving huge capital investments, high risk, long gestation and payback periods, and rapid changes in technology, which require significant and sustained investments.
- Minimal Fiscal Support from Government: The level of fiscal support currently envisioned is minuscule when one considers the scale of investments typically required to set up manufacturing capacities in the various sub-sectors of the semiconductor industry.
- Lack of Fabrication Capacities: India has a decent chip design talent but it never built up chip fab capacity. The ISRO and the DRDO have their respective fab foundries but they are primarily for their own requirements and are also not as sophisticated as the latest in the world.

- Extremely Expensive Fab Setup: A semiconductor fabrication facility (or fab) can cost multiples of a billion dollars to set up even on a relatively small scale and lagging by a generation or two behind the latest in technology.
- Resource Inefficient Sector: Chip fabs are also very thirsty units requiring millions of litres of clean water, an extremely stable power supply, a lot of land and a highly skilled workforce.
- Connectivity and Capability Related Measures: Many factors need to come together for India to make a mark in the niche chip-making and designing industry.
- High Investments Required: Semiconductors and display manufacturing is a very complex and technology-intensive sector involving huge capital investments, high risk, long gestation and payback periods, and rapid changes in technology, which require significant and sustained investments.

2.5 NEED TO ADDRESS RESEARCH AND DEVELOPMENT IN THE FIELD OF SEMICONDUCTORS AND MICROELECTRONICS

While efforts to advance current technology will continue, it is vital to undertake critical research in an array of areas beyond existing technology. For the semiconductor industry to continue achieving performance improvements, the broader research community needs a comprehensive approach that considers all aspects of semiconductor technology, including novel materials, new manufacturing techniques, new structures, systems architecture and applications. Future semiconductor-based systems—whether small sensors, high-performance computers, or systems in between—must maximize performance while minimizing energy use and providing security and assurance. The Semiconductor's industry vision has outlined the following areas in which research is essential to progress:

a. Advanced Devices, Materials, and Packaging

b. Interconnect Technology and Architecture

c. Intelligent Memory and Storage

d. Sensor and Communication Systems

e. Neuromorphic Computing

f. Environmental Health and Safety: Materials and Processes

g. Biomedical Applications

2.6. POTENTIAL AREAS OF RESEARCH AND ACTIVITIES PROPOSED TO BE UNDERTAKEN BY VDCoESM

The following research and activities are proposed to be undertaken by the VDCoESM on its establishment for achieving its objectives:

i. Establish a centralized state of the art infrastructure facility for next generation device design/materials research/fabrication in Semiconductor and Microelectronics
ii. Atomic-Scale/Nano-Scale Engineering of Semiconductor Materials and Devices
iii. Novel Approaches to Device Sensor Design: Biomedical Applications
iv. Novel Approaches to Device Sensor Design: Environmental Applications
v. Reliability of Semiconductor Logic and Memory Devices
vi. Introduction of short term courses
vii. Introduction of postgraduate and Ph.D. programs
viii. Offer internship, skill development and entrepreneurship program for diploma, undergraduate and postgraduate students, facilitate industrial training
ix. Development of a strong networking and collaboration with industries, research laboratories and institutions in India and abroad to carry out the cutting edge research and development

2.6.1. Establish a centralized state of the art infrastructure facility for next generation device design/materials research/fabrication in Semiconductor and Microelectronics

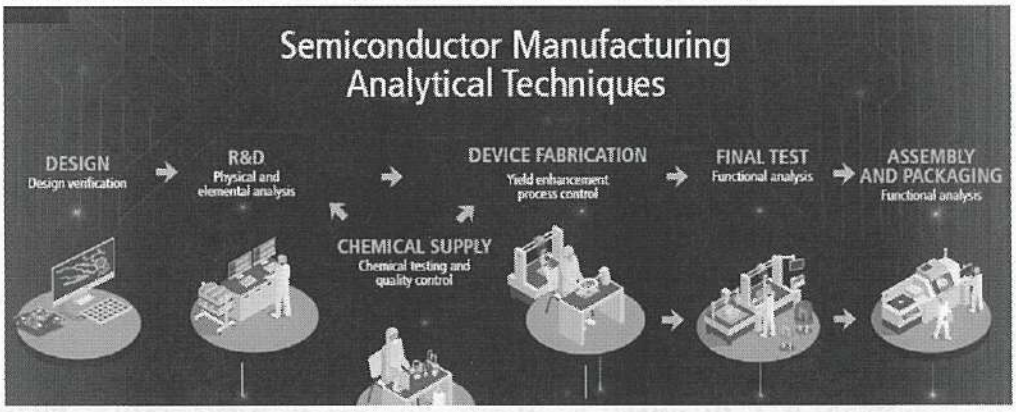
The new centre will focus on the research and development (R & D), engineering and testing of wafer fabrication hardware and software used in the creation of next generation of memory, sensing and logic technologies.

Heterogeneous integration of various functionalities, including sensing, neuromorphic, Optoelectronics, and Quantum technologies, is projected to be the driving force for industries in the coming decades. The projected future requirements demand technologies such as flexible & wearable electronics, bio-implantable & flexible neuromorphic processors, THz electronics, multi-dimensional sensors and sensory systems, and quantum-enhanced systems for computation, sensing, and communication. This has pushed stakeholders to think of universal technology platforms and better ways to meet future applications' needs.

Further, DTU has various semiconductor experts in different departments. They are working on various problems of divergent interests. A centre will be able to provide a point of convergence for experts to engage in community efforts in training and research. The Centre may have a topical research & training focus or a broader framework for semiconductors as a whole.

2.6.2. Atomic-Scale/Nano-Scale Engineering of Semiconductor Materials and Devices

Consumers are ever demanding smaller, lighter and safer electronic devices, which means semiconductors and electronic components must also shrink. Contaminants, even at ultra-trace levels will negatively impact the performance and reliability of the end product, which necessitates ultra-pure water, chemicals, gases, and solid materials. This infographic presents the analytical techniques and technologies which are utilized by semiconductor R&D managers to improve all areas of semiconductor, Integrated Circuitry and electronics manufacturing, from process development, process monitoring, QA/QC and failure testing, to assembly and packaging.



2.6.3 Novel Approaches to Device Sensor Design: Biomedical Applications

2.6.4. Novel Approaches to Device Sensor Design: Environmental Applications

2.6.5. Reliability of Semiconductor Logic and Memory Devices

It is well known that bit errors increase significantly as DRAM transistors are scaled below 28-32 nm node because the stored charge at the capacitor node and the leakage through the access transistor are sensitive to transistor scaling. Radiation-induced charge loss and gate leakage are concerns that must be addressed. Similarly, next-generation 3D NAND Flash memories will continue to grapple with read-margin, retention, and endurance issues arising from: (a) the threshold-voltage variation due to ambient temperature-sensitivity of polysilicon channel mobility, (b) threshold-voltage fluctuation due to trapping/de-trapping in the tunnel oxides, and (c) the reduced channel cross-section and enhanced field making the bottom cells susceptible to correlated HCI, TDDB, and radiation damages. There is an opportunity to develop more efficient ECC because the bit-flips in 3D NAND Flash are likely to be correlated.

2.6.6 Introduction of Short Term Courses

Short Term Courses on semiconductor chips and integrated circuits need to be introduced so that more design, development and manufacturing work is done in India and industries can take up the challenge to convert at a faster rate with the government support and research professionals.

2.6.7. Introduction of postgraduate (PG) and Ph.D. programs

Semiconductor chips form the backbone of the entire computing and electronic industry, healthcare, automobiles, military systems and countless other applications. Anything that plugs into a wall outlet requires at least one–if not many–semiconductor chips. Moreover, the semiconductor business has experienced shortages before, but the one that started because of the pandemic in March 2020 is much deeper. As global demand for semiconductor chips and integrated circuits increases, engineering expertise in semiconductors and microelectronics will become an even more valuable credential.

The programmes shall be offered in DTU that will help the expansion of the semiconductor industry by teaching cutting-edge technology for production of semiconductors chips and align the global demand for semiconductor chips with the industry

2.6.8. Offer internship, skill development and entrepreneurship program for diploma, undergraduate and postgraduate students, facilitate industrial training

Involvement of Industry Associations and Experts to ensure that the program deliverables meet the industry requirement, the industry experts will be involved at all the stages of the program. The experts will be made members of the Project Review and Monitoring Committee. Also, experts from the industry will also be involved in identification of SoC / system under the sub-activity 'Chip to System Development'. Moreover, students will be sent to leading Semiconductor MNCs (Intel/ NXP/ Cadence/Synopsys & S.T. Microelectronics) for Internship of 6 months to 1 year duration throughout the programme.

A Minor in Semiconductors and Microelectronics can be offered to Undergraduate/Postgraduate Students as follows:

Based on the Curriculum of Engineers, we have shortlisted few set of compulsory and elective courses that can be tagged as a Minor in Semiconductors and Microelectronics. The gap in the existing curriculum may be plugged by new course work. A minimum set of say 5 courses are required in the basket of Semiconductors and Microelectronics courses to qualify as a minor in Semiconductors and Microelectronics. These courses may include theory courses

and at least 2 practical/lab courses with hands-on experiments & training. Alternatively, a minimum of 5 courses with a mix of theory and labs or a significant project component may also count towards a Semiconductors and Microelectronics minor.

2.6.9. Development of a strong networking and collaboration with industries research laboratories and institutions in India and abroad to carry out the cutting edge research and development

The VDCoE4SM aims to collaborate with various industries and academic institutions involved in design, development, modelling and manufacturing of Semiconductor Chips in the country. Delhi Technological University has already/in process MoUs with following industrial partners working in different areas of semiconductor technology.

S.No.	MoUs Formulated/In Process	Departments Involved	Year of MoU
1.	ARIES, Nainital	Vinod Dham Centre of Excellence for Semiconductors and Microelectronics	In Process
2.	US Technology Pvt. Ltd, Bangalore	Vinod Dham Centre of Excellence for Semiconductors and Microelectronics	In Process

Key Benefits of the Collaboration between Delhi Technological University and Semiconductors/Microelectronics Industry is summarized as follows-

1. On-site and industry internships for students and faculty
2. Joint research projects and publications.
3. Joint Research and Development (R & D) relevant to future electronics devices with the involvement Semiconductor/Microelectronics Industry.
4. To conduct Inhouse/State and National Level Faculty Development Programs (FDPs), hands-on training and workshops in Custom IC design and wafer fabrication for faculty, technical staff and students.

3. REVIEW AND EVALUATION OF THE ACTIVITIES OF CoE

A **Monitoring Committee** will be formed for the mid term evaluation and progress of the performance of the CoE. The composition of the Monitoring Committee will be proposed in line with the composition as approved in 41st BOM Meeting held on March 01, 2021.

An **Advisory Committee** will be formed to oversee the initiation and implementation of various activities and programs at the CoE. The composition of the Advisory Committee will be proposed in line with the composition as approved in 41st BOM Meeting held on March 01, 2021.

4. CONCLUSION

The proposed centre will thus result in development of appropriate indigenous technologies for semiconductors and microelectronics to create a pool of trained manpower, provide training and internship to students and industry personnel transfer the developed technology to different industries and status for their commercialization and do grow along with in promotion and adaption of semiconductor chips in the country. As there is a need of Semiconductors as well as a global demand also to which India can cater to but that would require building upon the existing capabilities, putting robust policy mechanisms and ecosystems in place. It is also required for the industry and the government to work together. All these advantages have been there for a long time and it's now necessary to connect with them.

Annexure 35.10

Syllabus of Courses to be offered under Minor Specialization in Semiconductors and Microelectronics

ADVANCED WAFER PROCESSING

1. Subject Code: EPXXX : Course Title: Advanced Wafer Processing
2. Contact Hours : L: 3 T: 0/1 P: 2/0
3. Examination Duration (ETE)(Hrs.) : Theory: 3 Practical: 0
4. Relative Weightage : CWS:15/25 PRS:25/0 MTE:20/25 ETE:40/50 PRE:0
5. Credits : 4
6. Semester :
7. Subject Area : DEC
8. Pre-requisite : Nil
9. Objective : To provide an understanding of the manufacturing methods and their underlying scientific principles in the context of technologies used for VLSI chip fabrication.

S.No.	Contents	Contact Hours
1.	Crystal Growth, Wafer Preparation: Introduction & Historical Perspective, Clean room concept – Growth of single crystal Si, surface contamination, Chemical Mechanical Polishing, wafer preparation, DI water, RCA and Chemical Cleaning. Processing considerations: Chemical cleaning, getting the thermal Stress factors etc	6
2.	Epitaxy and Oxidation: Vapor Phase Epitaxy - Molecular Beam Epitaxy - Silicon on Insulators – Epitaxial Evaluation – Growth Mechanism and Kinetics – Thin Oxides – Oxidation Techniques and Systems – Oxide Properties.	6
3.	Lithography and Relative Plasma Etching: Optical Lithography – Electron Lithography – X-Ray Lithography - Ion Lithography Plasma - Properties – Feature Size - Control and Anisotropic Etch Mechanism – Relative Plasma Etching Techniques and Equipment.	9
4.	Deposition , Diffusion, Ion Implementation And Metallization: Deposition Processes – Polysilicon – Plasma Assisted Deposition – Models of Diffusion in Solids – Fick's One Dimensional Diffusion Equation – Atomic Diffusion Mechanism – Measurement Techniques – Range Theory – Implantation Equipment. Annealing Shallow Junction – High Energy Implantation – Physical Vapor Deposition – Patterning.	9
5.	VLSI Process Integration, Analytical, Assembly Techniques And Packaging of VLSI Devices: NMOS IC Technology – CMOS IC Technology – MOS Memory IC Technology – Bipolar IC Technology – IC Fabrication. Analytical Beams – Beams Specimen Interaction – Chemical Methods – Package Types baking Design Considerations – VLSI Assembly Technology – Package Fabrication Technology.	12
	TOTAL	**42**

Text Book/References:

1. S. M. Sze, Semiconductor Devices – Physics and Technology, 2nd Edition, Wiley, 2010.
2. Yannis Tsividis, Mixed Analog-Digital VLSI Device and Technology, World Scientific, 2002.
3. Yannis Tsividis, Operation and modeling of the MOS transistor, McGraw Hill, 1987.
4. S. M Sze, VLSI Technology, 2nd Edition, Tata McGraw Hill, 2003.

ADVANCED SEMICONDUCTOR DEVICE PHYSICS

1. Subject Code: EPXXX : Course Title: ADVANCED SEMICONDUCTOR DEVICE PHYSICS
2. Contact Hours : L: 3 T: 0/1 P: 2/0
3. Examination Duration (ETE)(Hrs.) : Theory: 3 Practical: 0
4. Relative Weightage : CWS:15/25 PRS:25/0 MTE:20/25 ETE:40/50 PRE:0
5. Credits : 4
6. Semester :
7. Subject Area : DEC
8. Pre-requisite : NIL
9. Objective : To introduce students to the physics of semiconductor devices and familiarize them with the internal mechanisms and phenomenons

S.No.	Contents	Contact Hours
1.	Crystal sructure, Electronic band structure, Elemental and compound (binary and ternary) semiconductors, Doping in semiconductors, Shallow and deep levels, Carrier statistics, Carrier transport, Carrier mobility, Scattering mechanisms, Hall effect measurements, High field property, Non-equilibrium conditions, Quasi Fermi levels, Recombination processes, Current density and continuity equations, Surface recombination, Surface states, Excitons in semiconductors.	10
2	Basic structure of pn junction, Zero applied bias: Electric field, built-in potential, junction capacitance, Current transport in pn junction diode, I-V characteristics, Small signal model of pn diode, Diffusion capacitance, Generation-recombination currents, Junction breakdown mechanisms. Heterojunctions: Band alignments, energy band diagrams of heterojunctions, formation of two dimensional electron gas.	10
3	Metal-semiconductor contacts: Schottky barrier diode, Energy band diagrams, Fermi level pinning, C-V characteristics of a Schottk diode, Current transport processes and I-V characteristics, Ohmic contacts.	8
4.	Ideal MOS structure, energy band diagrams under accumulation, depletion and inversion conditions, surface potential, flat band voltage and threshold voltage, variation of electric field and potential across a MOS structure, various types of charges in a MOS structure, some properties of silicon based MOS structures.	8
5.	MOSFET: Basic MOSFET structure, output and transfer characteristics, I-V relationships, nonideal effetcs in a MOSFET, CMOS technology.	6
	TOTAL	**42**

Text Book/References:

1. Y. Tsividis, Operation and Modeling of the MOS Transistor, Oxford University Press, (2008) 2nd ed.
2. S. M. Sze, Physics of Semiconductor Devices, Wiley (2008).
3. R. S. Muller, T. I. Kamins, and M. Chan, Device Electronics for Integrated Circuits, John Wiley (2007) 3rd ed.
4. Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press (2009).
5. G. Massobrio and P. Antognetti, Semiconductor Device Modeling, McGraw Hill (1998).

COMPACT MODELING AND PROCESS SIMULATION OF SEMICONDUCTOR DEVICES

1. Subject Code: EPXXX : Course Title: COMPACT MODELING AND PROCESS SIMULATION OF SEMICONDUCTOR DEVICES
2. Contact Hours : L: 3 T: 0/1 P: 2/0
3. Examination Duration (ETE)(Hrs.) : Theory: 3 Practical: 0
4. Relative Weightage : CWS:15/25 PRS:25/0 MTE:20/25 ETE:40/50 PRE:0
5. Credits : 4
6. Semester :
7. Subject Area : DEC
8. Pre-requisite : Fundamentals of semiconductor device physics
9. Objective : To introduce students to the field of compact modeling and familiarize them with the tools and methods used in industry-standard compact model development

S.No.	Contents	Contact Hours
1.	Introduction to modeling, key differences between different types of models, specific requirements for compact models, use and importance of compact models, familiarization with existing industry-standard compact models and their history.	2
2	Modeling Fundamentals: Mathematics required for compact modeling, maximum and minimum functions, various types of smoothing functions, continuity and differentiability, convergence criteria, numerical blow-ups, clamping functions, stitching functions, function choice, electrical equivalent circuits, handling differential equations, transient simulations, modeling methodology: semi-empirical, empirical, physical and look-up-table models.	5
3	Process Simulation and Coding: Process simulation basics, simulators, coding syntax and practices	3
4.	MOSFETs: Compact modeling of MOSFET electrostatics and transport, concept of core model, building a core model, add-on effects, short-channel effects, MOSFET charges, terminal currents and charges, parasitics, frequency dependence, MOSFET model types: surface potential based models, charge based models.	6
5.	Advanced Modeling Concepts: Binning, binning equations, instance parameters vs model parameters, macro definitions, backward-compatibility and incompatibility, speed/performance, accuracy, noise modeling, self-heating model, non-quasi-static model, quantum effects, band-structure effects, parasitics, ballistic transport, quasi-ballistic transport.	9

6	Advanced device effects: Study of industry-standard compact models: BSIMBULK,BSIM-CMG, BSIM-IMG, ASM-HEMT. Introduction to current devices (FinFETs, GAAFETs, FD-SOI,HEMTs) through case study. Discussion on problems encountered in modeling these devices along withsolutions adopted at present, scope for improvement	8
7.	Magnetic Devices: Compact modeling of STT-MRAM, concepts, key criteria for MTJ compact model,tunnel resistance model, switching model, performance criteria, key problems, scope for improvement.	3
8	Ferroelectric Devices: Compact modeling of ferroelectric materials and devices, NCFETs, L-K equation, domain picture, multi-domain modeling, switching model, MFMIS models vs MFIS models, current scenario, scope for improvement.	3
	TOTAL	**42**

Text Book/References:

1. Y. Tsividis and C. McAndrew, "Operation and Modeling of the MOS Transistor," Oxford Univ. Press
2. C. Hu, "Modern Semiconductor Devices for Integrated Circuits," Pearson.
3. Y. S. Chauhan et al., "FinFET Modeling for IC Simulation and Design: Using the BSIM-CMG standard," Academic Press.
4. C. Hu, "Industry Standard FDSOI Compact Model BSIM-IMG for IC Design," Woodhead publishing.
5. G. Gildenblat, "Compact Modeling: Principles, Techniques and Applications," Springer
6. W. Liu and C. Hu, "Bsim4 and Mosfet Modeling For Ic Simulation," World Scientific Publishing Co.
7. W. Liu, "MOSFET Models for SPICE Simulation: Including BSIM3v3 and BSIM4," Wiley-IEEE Press.

SEMICONDUCTOR OPTOELECTRONICS

1. Subject code: EPXX : Course Title: SEMICONDUCTOR OPTOELECTRONICS
2. Contact Hours : L:3 T:0/1 P:2/0
3. Examination Duration(ETE)(Hrs) : Theory:3 Practical:0
4. Relative Weightage : CWS: 15/25 PRS: 25/0 MTE:20/25 ETE:40/50 PRE:0
5. Credits : 4
6. Semester :
7. Subject Area : DEC
8. Pre-requisite : Solid State Physics, Semiconductor Physics, Electromagnetics
9. Objective : To introduce students to the physics of semiconductor optoelectronics and familiarise them with the internal mechanisms and phenomenons

S. No.	CONTENTS	CONTACT HOURS
1.	Energy bands in solids, density of states, occupation probability, fermi level, quasi fermi levels, semiconductor materials, interaction of light with electrons and holes in a semiconductor, carrier transport, semiconductor junctions, Optical Inter-band Transitions in Semiconductors	6
2.	**SEMICONDUCTOR LIGHT SOURCES (LEDs)** Light Emitting Diode: Basic Principles, Injection electroluminescence, Materials, Structure, Characteristics, Modulation Bandwidth, Applications	6
3.	**SEMICONDUCTOR LIGHT SOURCES-II (LASERS)** LASERS: Stimulated Emission, Population Inversion, Feedback, Laser Threshold, Laser Modes, Modulation Response, Applications, VCSELs, Quantum Well Lasers, DFB and DBR Structures	10
4.	**SEMICONDUCTOR PHOTODETECTORS** Rate of absorption in a semiconductor, materials, device structure, characteristics, power output, responsivity, speed of photodetector, PIN photodiode, APDs, Noise in Photodelectors, Applications	6
5.	**LIGHT MODULATORS AND PHOTOVOLTAIC DEVICES** Basic Principles, Electro-absorption Modulator: Device structure and Characteristics, Applications, Solar Cells: Device Physics, I-V characteristics in dark and light, Solar Energy Conversion, Conversion Efficiency, Materials, Applications	8
6.	**OPTOELECTRONIC INTEGRATED CIRCUITS** Introduction to OEICs, Design and Operation, Materials, Challenges, Hybrid Assembly, Modular Integration, Applications	6
	TOTAL	42

Text Book References:

1. Mitsuo Fukuda, Optical Semiconductor Device. ISBN: 978-0-471-14959-0, Wiley
2. S. O. Kasap, Optoelectronics and Photonics. ISBN-13: 978-0201610871, Prentice Hall, 2001
3. Coldren, and Corzine, Diode Lasers and Photonic Integrated Circuits. 1st ed. New York, NY: Wiley-Interscience, October 16, 1995. ISBN: 0471118753.
4. Chuang, S. L. Physics of Optoelectronic Devices. New York, NY: Wiley-Interscience, September 8, 1995. ISBN: 0471109398.
5. Shun Lien Chuang; Physics of Photonic Devices (2nd Edition; John Wiley & Sons (2009) ISBN-10: 0470293195; ISBN: 978-0470293195 (paperback)